TABOR ELECTRONICS

PROTEUS
Infinite possibilities

Proteus Series Arbitrary Waveform Generator/ Transceiver

Benchtop Model

User Manual

Rev. 1.2

Warranty Statement

Products sold by Tabor Electronics Ltd. are warranted to be free from defects in workmanship or materials. Tabor Electronics Ltd. will, at its option, either repair or replace any hardware products which prove to be defective during the warranty period. You are a valued customer. Our mission is to make any necessary repairs in a reliable and timely manner.

Duration of Warranty

The warranty period for this Tabor Electronics Ltd. hardware is one year, except software and firmware products designed for use with Tabor Electronics Ltd. Hardware is warranted not to fail to execute its programming instructions due to defect in materials or workmanship for a period of ninety (90) days from the date of delivery to the initial end user.

Return of Product

Authorization is required from Tabor Electronics before you send us your product for service or calibration. Call your nearest Tabor Electronics support facility. A list is located on the last page of this manual. If you are unsure where to call, contact Tabor Electronics Ltd. Tel Hanan, Israel at 972-4-821-3393 or via fax at 972-4-821-3388. We can be reached at: support@tabor.co.il

Limitation of Warranty

Tabor Electronics Ltd. shall be released from all obligations under this warranty in the event repairs or modifications are made by persons other than authorized Tabor Electronics service personnel or without the written consent of Tabor Electronics.

Tabor Electronics Ltd. expressly disclaims any liability to its customers, dealers and representatives and to users of its product, and to any other person or persons, for special or consequential damages of any kind and from any cause whatsoever arising out of or in any way connected with the manufacture, sale, handling, repair, maintenance, replacement or use of said products.

Representations and warranties made by any person including dealers and representatives of Tabor Electronics Ltd., which are inconsistent or in conflict with the terms of this warranty (including but not limited to the limitations of the liability of Tabor Electronics Ltd. as set forth above), shall not be binding upon Tabor Electronics Ltd. unless reduced to writing and approved by an officer of Tabor Electronics Ltd.

This document may contain flaws, omissions, or typesetting errors. No warranty is granted nor liability assumed in relation thereto. The information contained herein is periodically updated and changes will be incorporated into subsequent editions. If you have encountered an error, please notify us at support@taborelec.com. All specifications are subject to change without prior notice.

Except as stated above, Tabor Electronics Ltd. makes no warranty, express or implied (either in fact or by operation of law), statutory or otherwise; and except to the extent stated above, Tabor Electronics Ltd. shall have no liability under any warranty, express or implied (either in fact or by operation of law), statutory or otherwise.

Proprietary Notice

This document and the technical data herein disclosed, are proprietary to Tabor Electronics, and shall not, without express written permission of Tabor Electronics, be used, in whole or in part to solicit quotations from a competitive source or used for manufacture by anyone other than Tabor Electronics. The information herein has been developed at private expense, and may only be used for operation and maintenance reference purposes or for purposes of engineering evaluation and incorporation into technical specifications and other documents, which specify procurement of products from Tabor Electronics.

Table of Contents

List of Figures

List of Tables

Document Revision History

Revision	Date	Description	Author
1.2	20-Jan-2021	• 1.2 Software Support, page 15 – New. • Removed sections “Minimum System Requirements” and “Installation”. Refer to WDS User Manual. • Table 11.7 Direct Output (Optional), page 70 – Changed amplitude from 600 mVpp to “1 mVpp to 600 mVpp”.	Jakob Apelblat
1.1	28-Oct-2020	• Changed page size to letter. • 11.16 Digitizer Characteristics (AWT Option), page 74 – Changed Acquisition Memory from “<2 GS/channel” to “Up to max memory size”	Jakob Apelblat
1.0	24-Sep-2020	• Original release supporting WDS version 1.2.192, FPGA version 1.2.0	Jonathan Netzer

Acronyms & Abbreviations

Table Acronyms & Abbreviations

Acronym	Description
µs or us	Microseconds
ADC	Analog to Digital Converter
AM	Amplitude Modulation
ASIC	Application-Specific Integrated Circuit
ATE	Automatic Test Equipment
AWG	Arbitrary Waveform Generator
AWT	Arbitrary Waveform Transceiver
BNC	Bayonet Neill–Concelm (coax connector)
BW	Bandwidth
CW	Carrier Wave
DAC	Digital to Analog Converter
dBc	dB/carrier. The power ratio of a signal to a carrier signal, expressed in decibels
dBm	Decibel-Milliwatts. E.g., 0 dBm equals 1.0 mW.
DDC	Digital Down-Converter
DDS	Direct Digital Synthesis
DHCP	Dynamic Host Configuration Protocol
DSO	Digital Storage Oscilloscope
DUC	Digital Up-Converter
ENoB	Effective Number of Bits
ESD	Electrostatic Discharge
EVM	Error Vector Magnitude
FPGA	Field-Programmable Gate Arrays
GHz	Gigahertz
GPIB	General Purpose Interface Bus
GS/s	Giga Samples per Second
GUI	Graphical User Interface
HDMI	High-Definition Multimedia Interface
HP	Horizontal Pitch (PXIe module horizontal width, 1 HP = 5.08mm)

Acronym	Description
Hz	Hertz
IF	Intermediate Frequency
I/O	Input / Output
IP	Internet Protocol
IQ	In-phase Quadrature
IVI	Interchangeable Virtual Instrument
JSON	JavaScript Object Notation
kHz	Kilohertz
LCD	Liquid Crystal Display
LO	Local Oscillator
MAC	Media Access Control (address)
MDR	Mini D Ribbon (connector)
MHz	Megahertz
ms	Milliseconds
NCO	Numerically Controlled Oscillator
ns	Nanoseconds
PC	Personal Computer
PCAP	Projected Capacitive Touch Panel
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PRBS	Pseudorandom Binary Sequence
PRI	Pulse Repetition Interval
PXI	PCI eXtension for Instrumentation
PXIe	PCI Express eXtension for Instrumentation
QC	Quantum Computing
Qubits	Quantum bits
RADAR	Radio Detection And Ranging
R&D	Research & Development
RF	Radio Frequency
RMS	Root Mean Square
RT-DSO	Real-Time Digital Oscilloscope

Acronym	Description
s	Seconds
SA	Spectrum Analyzer
SCPI	Standard Commands for Programmable Instruments
SFDR	Spurious Free Dynamic Range
SFP	Small Form-Factor Pluggable
SFP	Software Front Panel
SMA	Subminiature version A connector
SMP	Subminiature Push-on connector
SPI	Serial Peripheral Interface
SRAM	Static Random-Access Memory
TFT	Thin Film Transistor
T&M	Test and Measurement
TPS	Test Program Sets
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus
VCP	Virtual COM Port
Vdc	Volts, Direct Current
V p-p	Volts, Peak-to-Peak
VSA	Vector Signal Analyzer
VSG	Vector Signal Generator
WDS	Wave Design Studio

1 General

1.1 Scope

The scope of this manual is to describe the setup and operating procedures of the Tabor Electronics Proteus Benchtop series.

1.2 Software Support

Proteus Benchtop comes with a powerful CPU with Windows 10 installed that runs the Tabor Wave Design Studio (WDS) for control and operation of the benchtop. **WDS** can also be installed on a control PC for convenient remote control of Proteus. Use the **TE Update Tool** to update the Proteus device FPGA. The programs and the user manual can be downloaded from the Tabor Electronics website at http://www.taborelec.com/downloads.

1.3 Document Conventions

1.3.1 General

Convention	Description	Example
Bold Writing	Indicates an item/message in the User Interface.	Click the **On** button.
<Angled and Bolded Brackets>	Indicates a physical key on the keyboard.	Press <Ctrl>+<B>.

Caution!

- A Caution indicates instructions, which, if not followed, may result in damage to the equipment or to the loss of data.

Note

- A Note provides additional information to help obtain optimal equipment performance.

Idea

- An Idea provides an alternate procedure to obtain the same results.

1.3.2 Programming

Convention	Description	Example
{}	Braces indicate that parameters may be used in the command once, or several times, or not at all.	:LIST:POWer <val>{,<val>} a single power listing: LIST:POWer 5 a series of power listings: LIST:POWer 5,10,15,20
<>	Angle brackets indicate that their contents are not to be used literally in the command. They represent the required parameters.	:FREQuency:STARt <val><unit> In this command, the words <val> and <unit> should be replaced by the actual frequency and unit. :FREQuency:STARt 2.5GHZ
[]	Square brackets indicate that the enclosed keywords or parameters are optional when composing the command. The commands will be executed even if they are omitted.	:FREQuency[:CW]? SOURce and CW are optional items.
|	A vertical stroke between keywords or parameters indicates alterative choices. For parameters, the effect of the command varies depending on the choice.	:AM:MOD DEEP|NORMal DEEP or NORMal are the choices.

1.4 Safety

To avoid electrical shock, fire, or personal injury:

- Use only the proper power cord and certified for the country of use.
- This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, the grounding conductor must be connected to the ground. Before connecting to the power input or output, ensure that the product is properly grounded.
- Do not operate this product with removed covers or panels.
- Observe all the ratings and markings on the product. Search this manual for further rating information, before connecting to it. Do not apply potential that is higher than the maximum rating.
- Do not operate in dark or wet conditions.
- Do not operate in an explosive environment. Keep product clean and dry.

1.5 Maintenance

1.5.1 Preventive Maintenance

There are no hardware adjustments within Proteus Generators. Tabor Electronics recommends that the Proteus Generator is calibrated every 24 months or whenever a problem is suspected. The specific calibration interval depends upon the accuracy required. No periodic preventive maintenance is required.

1.5.2 Long Term Storage or Repackaging For Shipment

If the instrument is to be stored for a long period of time or shipped immediately, proceed as directed below. If you have any questions, contact your local Tabor Electronics representative or the Tabor Electronics Customer Service Department.

1. Repack the instrument using the wrappings, packing material and accessories originally shipped with the unit. If the original container is not available, purchase replacement materials.
2. Be sure the carton is well sealed with strong tape or metal straps.
3. Mark the carton with the model and serial number. If it is to be shipped, show sending and return address on two sides of the box.

   If the instrument is to be shipped for service or repair, the following information must be included with the shipment:

   - Name and address of the owner.
   - Record the model and serial number of the instrument, options, and firmware version.
   - Note the problem and symptoms – detailed information will help in verifying the problem
     - What was the instrument setup?
     - Did the unit work; then fail?
     - What other equipment was connected to the generator when the problem occurred?

- The name and telephone number of someone familiar with the problem who can be contacted by Tabor Electronics if any further information is required.
- Show the returned authorization order number (RMA) as well as the date and method of shipment.

Note

Always obtain a return authorization number from the factory before shipping the instrument to Tabor Electronics.

2 Introduction

2.1 Overview

This manual provides a detailed functional description for the Tabor Electronics Proteus Benchtop series. Proteus is a series of arbitrary waveform generators and transceivers that transmit, receive, and perform digital signal processing all in a single instrument with various sampling rate options. The Proteus Benchtop is a fully standalone operated system. The manual covers the following models listed in the below ordering information. For a list of options refer to Table 2.2 Available Options for Proteus Benchtop, page 19

Table 2.1 Ordering Information

Model	Description
P1282B	1.25 GS/s, 16 bit, AWG, 1 GS memory, 2 channels, 4 markers
P1284B	1.25 GS/s, 16 bit, AWG, 1 GS memory, 4 channels, 4 markers
P1288B	1.25 GS/s, 16 bit, AWG, 2 GS memory, 8 channels 8 markers
P12812B	1.25 GS/s, 16 bit, AWG, 2 GS memory, 12 channels 12 markers
P2582B	2.5 GS/s, 16 bit, AWG, 2 GS memory, 2 channels, 8 markers
P2584B	2.5 GS/s, 16 bit, AWG, 2 GS memory, 4 channels, 8 markers
P2588B	2.5 GS/s, 16 bit, AWG, 2 GS memory, 8 channels 16 markers
P25812B	2.5 GS/s, 16 bit, AWG, 2 GS memory, 12 channels, 24 markers
P9082B	9 GS/s, 16 bit, AWG, 4 GS memory, 2 channels, 8 markers
P9084B	9 GS/s, 16 bit, AWG, 4 GS memory, 4 channels, 16 markers
P9086B	9 GS/s, 16 bit, AWG, 4 GS memory, 6 channels, 24 markers

Figure 2.1 Proteus Benchtop P25812B

2.2 Features and Highlights

- Dual, four, eight or twelve channel 1.25 GS/s & 2.5 GS/s 16 bit, or dual, four or six channel 9 GS/s 16 bit, AWG & AWT (Arbitrary Waveform Generator/Transceiver) configurations
- Integrated NCO (Numerically Controlled Oscillator) for digital upconverting to microwave frequencies
- Real time data streaming directly to the FPGA for continuous and infinite waveform generation
- 8 GHz bandwidth, 5.4 GS/s 12-bit single and dual digitizer option for feedback control system and conditional waveform generation
- Innovative task-oriented sequence programming for maximum flexibility to generate any imaginable scenario
- Excellent phase noise and spurious performance
- User customizable FPGA for demodulation, digital filtering, and application specific solutions
- Standalone 4U, 19” wide benchtop platform, with 9” touch display, USB 3.0, 10G Ethernet and Thunderbolt high speed interfaces
- Up to 16 GS waveform memory with the ability to simultaneously generate and download waveforms

2.3 Options

The Proteus Benchtop can be ordered with the following options.

Table 2.2 Available Options for Proteus Benchtop

Option	Description	Model
4M1	4 GS memory	P1282B, P2582B
4M2	4 GS memory	P1284B, P2584B
4M3	4 GS memory	P1288B, P2588B, P9084B
4M4	4 GS memory	P12812B, P25812B, P9086B
8M1	8 GS memory	P1282B, P2582B
8M2	8 GS memory	P1284B, P2584B, P9082B
8M3	8 GS memory	P1288B, P2588B, P9084B
8M4	8 GS memory	P12812B, P25812B, P9086B
16M1	16 GS memory	P9082B
16M2	16 GS memory	P9084B
16M3	16 GS memory	P9086B
DO1	9 GHz BW direct output	P1282B, P2582B
DO2	9 GHz BW direct output	Pxx84B, P9082B

DO3	9 GHz BW direct output	Pxx88B, P9084B
DO4	9 GHz BW direct output	Pxx812B, P9086B
DJ1	Dynamic jump control	P1282B, P2582B
DJ2	Dynamic jump control	P1284B, P2584B, P9082B
DJ3	Dynamic jump control	P1288B, P2588B, P9084B
MRK1	x8 extra markers	P1282B, P2582B
MRK2	x8 extra markers	P1284B, P2584B, P9082B
MRK3	x16 extra markers	P1288B, P2588B, P9084B
LTJ1	Ultra-low trigger jitter (200 ps typ.)	P1282B & P2582B
LTJ2	Ultra-low trigger jitter (200 ps typ.)	P1284B, P2584B, P9082B
LTJ3	Ultra-low trigger jitter (200 ps typ.)	P1288B, P2588B, P9084B
LTJ4	Ultra- low trigger jitter (200 ps typ.)	P12812B, P25812B, P9086B
G1	Low waveform granularity	P1282B, P2582B
G2	Low waveform granularity	P1284B, P2584B, P9082B
G3	Low waveform granularity	P1288B, P2588B, P9084B
G4	Low waveform granularity	P12812B, P25812B, P9086B
AWT	5.4 GS/s Single, 2.7 GS/s dual channel 12-bit digitizer	P1284B, P1288B, P2584B, P2588B, P9082B, P9084B
STM	3 GS/s streaming	
PROG	High level FPGA programming capability through decision blocks of built-in demodulation & digital filters	
Shell	Open core integration to allow simple FPGA control & programming	
TBolt	Rear-panel Thunderbolt 3 (USB-C connector)	
SFP+	Rear-panel 10 G optical SFP+ (replaces the RJ45)	

Option M – This option offers to increase the standard waveform memory of the unit as detailed in the table below:

Table 2.3 Memory Configuration and Options

Model	Strd.	4M1	4M2	4M3	4M4	8M1	8M2	8M3	8M4	16M1	16M2	16M3
P1282B	1 GS	4 GS				8 GS						
P1284B	1 GS		4 GS				8 GS					
P1288B	2 GS			4 GS				8 GS				
P12812B	2 GS				4 GS				8 GS			
P2582B	2 GS	4 GS				8 GS						

P2584B	2 GS		4 GS				8 GS					
P2588B	2 GS			4 GS				8 GS				
P25812B	2 GS				4 GS				8 GS			
P9082B	4 GS						8 GS			16 GS		
P9084B	4 GS			4 GS				8 GS			16 GS	
P9086B	4 GS				4 GS				8 GS			16 GS

Option DO – There are two available output configurations:

1. Direct Output (DO): This is a direct AC coupled output without an amplifier and is optimized for maximum analog BW as well as best SFDR (Spurious Free Dynamic Range). It offers a programmable amplitude range of 400 mVpp to 600 mVpp.
2. DC Output: This is the default configuration. A DC coupled output amplifier offering up to 1.3 Vpp with a voltage window of ±1.15 V.

Option DJ – The Dynamic jump offers the capability of switching segments through an external MDR connector. Refer to 12 Appendix , page 77 for the MDR connector pin description.

Option MRK – This option provides 8 additional markers.

Option LTJ – This option improves Proteus trigger jitter to a fixed 200 ps independent of the SCLK setting.

Option G – This option increases the segment resolution to 32 points.

Option PROG – This option enables the user to use built in digital processing library blocks such as demodulators, filters, and math functions as part of the signal processing chain without FPGA programming knowledge.

Option Shell – This option is for users with advanced FPGA programming knowledge in Xilinx Vivado Design Suite. The Proteus is supplied only with the necessary communications and data transfer cores and enables the user to implement their own IP on the available resources of the FPGA.

2.4 Front Panel Controls

Figure 2.2 P25812B Front Panel

Note

- The front panel control buttons will be disabled if a PC running WDS is controlling the device.

- **Power Button**  – Turn on/off the device.
- **9" Touch LCD Display** – 1024x 600 TFT display PCAP (Projected Capacitive Touch Panel) touch screen for controlling the device.
- **Home** – Open the WDS wave composer screen.
- **Keyboard** – Open/close the on-screen keyboard.
- **Touch** – Enable/disable the touch display.
- **Store** – Store current settings on selected memory device. Click the button to display a list of setting files, use the dial to scroll the list and push then the dial to store the settings in the file.
- **Recall** – Recall stored configuration.
- **System** – Display the WDS System screen.
- **SCLK** – Display the WDS sample clock parameter settings for editing.
- **Standard** – Display the WDS standard waveform screen.
  - **In Standard Mode** – A prompt message to the user.
  - **Not in Standard Mode** – Focus on SCLK textbox.
- **AMPT** – Display the WDS amplitude parameter settings for editing.
- **Arbitrary** – Display the WDS Scenario Composer screen and select the Arbitrary function mode.
- **Run Mode** – Display the WDS Control screen.
- **OFFSET** – Display the WDS offset parameter settings for editing.
- **TASK** – Display the WDS Scenario Composer screen and select the Task function mode.
- **Markers** – Display the WDS Wave Composer screen and open the Marker window pane.
- **Preset** – Restore to factory defaults.
- **CH1…CH12 –** Select the channel, 1 up to 12 depending on model, to show on the display. First click will make this channel the active channel and the second click will activate the output. The third click will de-activate the output.
- **Numeric Keypad** – Enter numeric values.
- **G/n Button** – Select GSa/s for SCLK.
- **M/µ Button** – Select MHz, µsec or µV units depending on selected parameter. Not implemented yet.
- **k/m Button** – Select mV for Amplitude/Offset.

- **x1 Button** – Select x1 (default unit) or dBm units depending on selected parameter.
- **Back** – The backspace key deletes the last entered character.
- **Esc** – Has two functions:
    1. When in edit mode, cancels edit operation, restores last value, and returns to the main function screen.
    2. When operating the device from a remote interface, none of the front panel buttons are active except the Local button. When pressed, it restores control to front panel buttons.
- **Enter** –
    1. When multiple parameters are displayed on the screen, the cursor and the dial scroll through the parameters. Pressing Enter selects the parameter for edit. After the parameter has been modified, the Enter button locks in the new variable and releases the buttons for other operations.
    2. When a parameter is modified, Enter can be used to replace the x1 suffix key.
    3. When a discrete parameter is selected, Enter toggles between the values.
- **Man Trigger** – Manual trigger button, used instead of an external trigger signal.
- **Dial** – Turning the dial clockwise or counterclockwise works like the arrow UP and Down keys. Pushing the dial works like the Enter button.
- **Arrow Up, Down, Left, Right** – Has two functions:
    1. When multiple parameters are displayed on the screen, the arrow and the dial scroll through the parameters.
    2. When a parameter is selected for editing, arrow buttons right or left move the cursor accordingly. Arrow buttons up or down modifies parameter value accordingly.

2.5 Front Panel Connectors

The front panel of the Proteus device varies according to the device model and configuration. However, regardless of the configuration, all connector types follow the same principle. All high-frequency analog output and input connectors are of SMA type. All low-frequency analog output and input connectors as well as all digital output and input connectors are of SMP type.

Figure 2.3 P25812B Front Panel with 12 Channels

- **USB Host** – USB 3 Type A interface for connecting a USB device such as a memory device (FAT32) for storing and recalling instrument setups, keyboard, or mouse.

- **CH1/…12/ –** There are two SMA connectors for each channel output, normal (top) and inverted (bottom) outputs. The output source impedance is 50 Ω (100 Ω when connected differentially), therefore the cable connected to this output should be terminated with a 50 Ω load resistance. For different load resistance, determine the actual amplitude from the following equation:

$$V_{out} = 2V_{prog}\left(\frac{R_{load}}{50 + R_{load}}\right)$$

The output amplitude is doubled when the load impedance is above roughly 10 kΩ. Also, the output can be turned on and off. However, turning the output off stops the signal, but leaves low impedance on the output terminals.

> **Note**
> When using the outputs as single ended it is necessary to use a 50 Ω termination on the inverted output to prevent any distortion on the output signal.

- **CLK IN –** The sample clock in SMA connector accepts an external signal that will replace the internal sample clock generator. This input, accepts signals covering the instrument's entire sample clock range, with an input level range of 0 V to 1 V. The output impedance of this connector is 50 Ω and it is AC coupled. The sample clock input is active only after selecting the external SCLK source option.

- **CLK OUT –** The sample clock out SMA connector outputs the internal sample clock generator or the external SCLK if an external sample clock is used. The sample clock out signal covers the entire sample clock range, with an output amplitude of 0.5 V to 1 V depending on the frequency. The output impedance of this connector is 50 Ω and it is AC coupled.

- **REF IN –** The reference in SMP connector accepts signals of either 10 MHz or 100 MHz. This input is normally used for synchronizing system components to a single clock reference. The Proteus device must be programmed to the reference frequency value and placed in external reference mode before it will use this input as reference.

- **REF OUT –** The reference out SMP connector outputs the 100M Hz internal reference (square waveform) or if using an external reference, the Ref Out outputs the external reference frequency. This output can be used to synchronize other system components to the Proteus clock reference.

> **Benchtop Synchronization TBD**
> When synchronizing multiple benchtops, the benchtops need to be daisy chained between REF OUT to REF IN. Therefore, in this mode the REF OUT is available only for synchronization. The REF IN of the master benchtop unit can accept an external reference signal, and all benchtops will be synchronized to this reference signal.

- **TRIG 1/2/3/4/5/6 –** There are between 2 to 6 trigger inputs depending on the Proteus model. In general, the trigger inputs are used to initiate or abort waveform generation. In arbitrary mode this is used to start or stop a current segment from playing. In task mode this can also be used as a condition signal for how to progress in the task table. The trigger input is inactive when the generator is in continuous operating mode. When placed in trigger mode, the trigger input is made active and waits for the right condition to trigger the instrument. Trigger level and edge sensitivity are programmable for the trigger input. For example, if your trigger signal rides on a DC level, you can offset the trigger level to the same level as your trigger signal, thus assuring the correct threshold for the trigger signal. The trigger level is adjustable from -5 V to +5 V. The programmed trigger level is common for all channels. All other trigger parameters including trigger state, are independent and can programmed per channel. The trigger input connectors are of SMP type. By default, the input impedance is 50 Ω but can be factory configured to 10 kΩ when ordered.

- **CH1…12 M1…M4 –** There are between 1 to 4 output markers available for each analog channel output depending on the Proteus model. The markers are generated through SMP connectors and are marked with the channel number they are associated to, and the marker number e.g. CH1 M1 is Marker 1 of Channel 1. Markers can be programmed from remote to create complex digital patterns. Waveform data and marker data are downloaded separately, however each waveform segment has a dedicated marker segment of equal length. Markers output has an output impedance of 50 Ω and marker level can be programmed up to 1.2 Vpp.

- **SYNC CLK –** This SMP connector outputs a clock signal, that is a division of the device sampling clock. For the 9 GS/s Proteus models the sampling clock is divided by 32 and for all other models it is divided by 8. When this signal is used as the sampling clock for an external triggering unit the resulting trigger jitter of the Proteus device will be ~0 ps.

- **Dynamic Control1/2/3** – Option DJ1/2/3. dynamic jump control input with a D-SUB 9-Pin connector. Refer to 12 Appendix D-Sub, page 77.

2.6 Rear Panel Connectors

Figure 2.4 Rear Panel

- **USB Host** – 2 x USB 3 Type A interface for connecting a USB device such as a memory device (FAT32) for storing and recalling instrument setups, keyboard, or mouse.
- **LAN RJ45** – RJ45 1000BaseT Ethernet connector for connecting a control PC via the LAN.
- **SFP** – Optional factory installed. The 10 G optical SFP replaces the RJ45.
- **HDMI** – HDMI Type A for connecting an external display.
- **USB Device** – USB 3 Type C for connecting a control PC.
- **Thunderbolt** – Optional factory installed. Thunderbolt 3 high speed interfaces.
- **GPIB** – Optional factory installed. Interface for connecting a legacy control PC.
- **AC Power Socket** – 3 Pins IEC320 C14 Inlet Power Plug Socket.

3 Installation

3.1 Installation Overview

This chapter contains information and instructions necessary to prepare the Proteus device for operation. Details are provided for initial inspection, grounding safety requirements, repackaging instructions for storage or shipment, and installation information.

3.2 Unpacking and Initial Inspection

Unpacking and handling of the device requires normal precautions and procedures applicable to handling of sensitive electronic equipment. The contents of all shipping containers should be checked for included accessories and certified against the packing slip to determine that the shipment is complete.

The Proteus Benchtop is supplied with:

- Power cord with a plug according to customer country standard.
- USB Type C cable for connecting a control PC to the instrument.
- CD with WDS software, user manuals and instrument drivers.

Caution!
The Proteus Benchtop ships in an antistatic package to prevent damage from electrostatic discharge (ESD). When storing the unit, use the antistatic case.

3.3 Safety Precautions

This product is intended for use by qualified persons who recognize shock hazards and are familiar with the safety precautions required to avoid possible injury. The following sections contain information and cautions that must be observed to keep the device operating in a correct and safe condition.

Caution
For maximum safety, do not touch the product, test cables, or any other instrument parts while power is applied to the circuit under test. ALWAYS remove power from the entire test system before connecting cables or jumpers, installing, or removing cards from the chassis. Do not touch any object that could provide a current path to the common side of the circuit under test or power line (earth) ground. Always keep your hands dry while handling the instrument.

Caution
Always keep the lid closed when power is applied to the device under test conditions. Carefully read the Safety Precautions instructions that are supplied with your test fixtures. Any adjustment, maintenance and repair of an opened, powered-on instrument must be performed by authorized service personnel.

3.4 Operating Environment

The device is intended for indoor use and should be operated in a clean, dry environment with an ambient temperature within the range of 0°C to 40°C.

> **Warning**
> The Proteus device must not be operated in explosive, dusty, or wet atmospheres. Avoid installation of the module close to strong magnetic fields.

The design of the device has been verified to conform to EN 61010-1 safety standard per the following limits: Installation (Overvoltage) Category I (Measuring terminals) Pollution Degree 2 Installation (Overvoltage) Category I refers to signal level, which is applicable for equipment measuring terminals that are connected to source circuits in which measures are taken to limit transient voltages to an appropriately low level. Pollution Degree 2 refers to an operating environment where normally only dry non-conductive pollution occurs. Occasionally a temporary conductivity caused by condensation must be expected.

3.5 Power Requirements

The waveform generator may be operated from a wide range of mains voltage from 100 to 264 VAC. Voltage selection is automatic and does not require switch setting. The instrument operates over the power mains frequency range of 47 to 63Hz. Always verify that the operating power mains voltage is the same as that specified on the rear panel. The instruments power consumption is 550 W max.

The device should be operated from a power source with neutral or near ground (earth potential). The instrument is not intended for operation from two phases of a multi-phase ac system or across the legs of a single-phase, three-wire AC power system. Crest factor (ratio of peak voltage to RMS) should be typically within the range of 1.3 to 1.6 at 10% of the nominal RMS mains voltage.

3.6 Grounding Requirements

To ensure the safety of operating personnel, the U.S. O.S.H.A. (Occupational Safety and Health) requirement and good engineering practice mandate that the instrument panel and enclosure be “earth” grounded. Although BNC housings are isolated from the front panel, the metal part is connected to earth ground.

> **Caution**
> Do not attempt to float the output from ground, as it may damage the device and your equipment.

3.7 Calibration

The recommended calibration interval is two years. Calibration should be performed by qualified personnel only.

3.8 Performance Checks

The device has been inspected for mechanical and electrical performance before shipment from the factory. It is free of physical defects and in perfect electrical order. Check the instrument for possible damage in transit and perform the electrical procedures outlined in the section entitled Unpacking and Initial Inspection.

3.9 Long Term Storage or Repackaging for Shipment

If the instrument is to be stored for a long period of time or shipped immediately, proceed as directed below. If you have any questions, contact your local Tabor Electronics representative or the Tabor Electronics customer service department.

1. Repack the instrument using the wrappings, packing material and accessories originally shipped with the unit. If the original container is not available, purchase replacement materials.
2. Be sure the carton is well sealed with strong tape or metal straps.
3. Mark the carton with the model and serial number. If it is to be shipped, show sending and return address on two sides of the box.

Note
If the instrument is to be shipped to Tabor Electronics for calibration or repair, attach a tag to the instrument identifying the owner. Note the problem, symptoms, and service or repair desired. Record the model and serial number of the instrument. Show the returned material authorization (RMA) order number as well as the date and method of shipment. Always obtain an RMA number from the factory before shipping the instrument to Tabor Electronics.

3.10 Preparation for Use

Preparation for use includes removing the instrument from the container box, installing the software, and connecting the cables to its input and output connectors.

3.10.1 Installation

If the intention is to mount the instrument in a rack, it must be installed in a way that clears air passage to its cooling fans. For inspection and normal bench operation, place the instrument on the bench so it is clear of any obstructions to the rear/bottom fan, to ensure proper airflow.

Warning
Once the device is installed in the chassis cover all remaining open slots to ensure proper airflow. Using the device without proper airflow will result in damage to the instrument. It is also recommended to use the highest fan setting available on the chassis to ensure proper cooling of the Proteus device.

3.10.2 Installing Instrument Drivers

The Proteus device is supplied with a CD that contains all the necessary installation drivers, control

software and relevant documentation. Follow the instructions below to install all the necessary drivers and DLLs on your PC to communicate and control you Proteus device. Refer also to 14.1 Manually Installing Instrument Drivers, page 79.

Note
Check the Tabor Electronics website for the most recent software, driver, firmware, and documentation updates. www.taborelec.com/downloads.

3.11 Multi Instrument Synchronization TBD

There are applications that require more than the 2 to 12 channels that a single Proteus Benchtop can offer. This is where the scalability of the Proteus Benchtop platform can be utilized. Multiple benchtops can be synchronized to create a multi-channel system. The procedure is described in the following paragraphs.

3.11.1 Master Slave Operation

When synchronizing multiple benchtops, one is designated as the master and the rest as slaves. The master benchtop provides the system clocks and necessary triggers to synchronize and align all of the benchtops.

3.11.2 Connecting the Instruments

Once all the benchtops have been placed one next to the other, they now need to be cross connected with the designated SMP to SMP synchronization cable. Locate the REF OUT connector of the master instrument (left most benchtop) and attach one end of the cable. Next, connect the other end of the cable to the REF IN connector of the adjacent slave 1 benchtop. Continue daisy chaining from slave 1 REF OUT to slave 2 REF IN and so on until all benchtops have been connected.

3.11.3 Operating Synchronized Instruments

When operating two or more synchronized instruments, there are some important limitations to be familiar with in order to achieve optimal performance.

1. Instruments and cables must be placed and connected as described in previous paragraphs.
2. Synchronization mode must be activated either from Wave Design Studio or by SCPI command.
3. Synchronization and channels alignment is automatic.
4. Manual alignment can be performed to improve the skew between channels.
5. Sample clock change is implemented in the master unit alone. Any SCLK change command to one of the slave units will automatically result in the unit exiting from the synchronization mode.
6. Other than SCLK change, each instrument can be independently programmed with a unique set of waveforms, segment table, task table, amplitude, offset, and markers.

4 Wave Design Studio (WDS)

Proteus Benchtop comes with a powerful CPU with Windows 10 installed that runs the Tabor Wave Design Studio (WDS) for control and operation of the benchtop. WDS will be invoked on power up of the device. Refer to the Wave Design Studio (WDS) User Manual that can be downloaded from the Tabor website at www.taborelec.com/downloads.

5 Understanding the Instrument

5.1 Introduction

This section provides a description of the features and functions available in the Proteus benchtop series of arbitrary waveform generators/transceivers.

5.2 General Description

The Proteus benchtop series is a multi-channel arbitrary waveform generator and transceiver. It is designed to offer outstanding performance with new and advanced capabilities and all this in a compact, standalone platform. Incorporating the most advanced and cutting-edge technology assures that the Proteus series, is and will be for many years to come, the ideal signal source for many applications.

The benchtop platform offers five different models depending on the SCLK speed and number of channels. The model numbering scheme for the entire Proteus series is shown in the figure below:

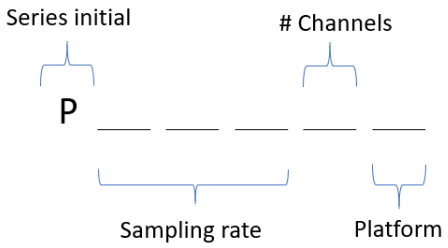

Figure 5.1 Proteus Model Numbering

Example
Model P2582B is a Proteus series model, with a 25 x 10^8 samples per second (2.5 GS/s) sampling rate and 2 output channels based on the benchtop platform.

The following table summarizes the available Proteus benchtops.

Table 5.1 Proteus Benchtop vs. GS/s

Sample Rate / Channel Count	1.25 GS/s	2.5 GS/s	9 GS/s
2 Channels	P1282B	P2582B	P9082B
4 Channels	P1284B	P2584B	P9084B
6 Channels			P9086B
8 Channels	P1288B	P2588B	
12 Channels	P12812B	P25812B	

5.3 System Overview

The Proteus Benchtop system is comprised of anywhere between 1 to 3 Proteus Modules. The following description and block diagram below refer to a single module and depicts the core of the system without any special options.

The Proteus system is an AWG (Arbitrary Waveform Generators) module, occupying 2 PXIe (PCI Express eXtension for Instrumentation) slots. The main board (Part 1) comes with one DAC (Digital to Analog Converter) and a mezzanine card (Part 2) provides an additional DAC. The DAC can provide one or two output channels depending on the DAC version.

The 9 GS/s 2 channel instrument utilizes a single-channel DAC while all other models use a dual-channel DAC. The 1.25GS/s and 2.5GS/s dual-channel instruments does not have any mezzanine card.

There is a DDR4 module for each DAC containing all the wave data, markers data, as well as the task, scenario, and segment tables.

System timing and data is controlled through a single FPGA and the communication interface to an external PC is done through 8 lanes of PCIe GEN3.

Note

In the Benchtop platform the communication interface is limited to 4 lanes of PCIe GEN3

Various HW options can be added to the AWG module, such as a digitizer, 8 extra digital markers and fast segment dynamic jump. Each of these options adds an additional PCB board that occupies an additional PXI slot.

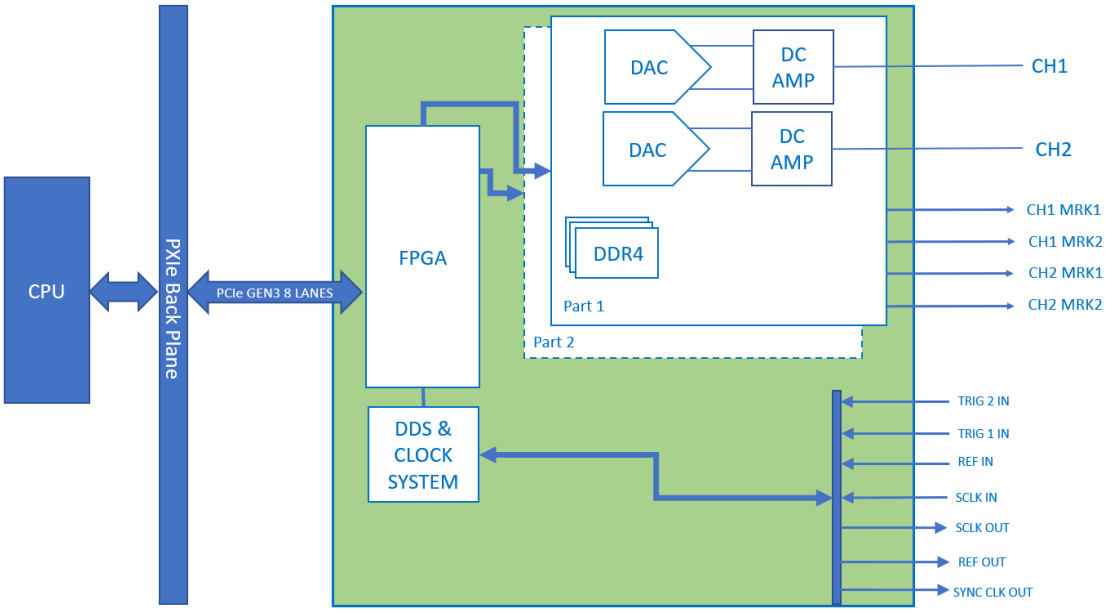

Figure 5.2 Proteus Block Diagram

5.4 Modes of Operation

There are four modes that can be used in order to generate a signal with the Proteus AWG. Direct mode, NCO mode, IQ mode and Streaming mode. An explanation on each of the modes follows.

5.4.1 NCO Mode

The NCO mode utilizes the integrated Numerically Controlled Oscillator (NCO) to generate sine waveforms. In this mode the arbitrary waveform memory is not used. The frequency generated can be set from DC to 40% of the SCLK setting. Each channel has an independent NCO that can generate a different frequency.

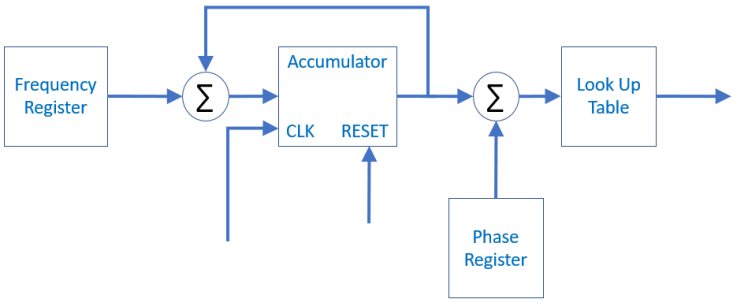

Figure 5.3 NCO Block Diagram

5.4.2 IQ Mode

The Proteus AWG generation capabilities include a wide band digital up-converter, or a wide-DUC (Digital Up-Converter). When using the IQ Mode, the waveform stored in the waveform memory is mixed with the NCO to generate an AM modulated waveform where the carrier waveform is generated by the NCO.

5.4.3 Streaming Mode

When generating arbitrary waveforms, the amount of data that can be generated is limited by the amount of onboard waveform memory that is available. In addition, it requires having the data prepared in advance and loaded to the waveform memory before generation. The streaming mode of the Proteus AWG enables the user to “by-pass” the on-board waveform memory and continuously generate signals by streaming the waveform straight from the controlling PC, whether from a large file or a real time generation of the data. When using the streaming mode, the sampling rate of the data is limited by the system data transfer rate. The overall sample rate cannot exceed the data transfer rate.

5.5 Channel Outputs

The Proteus AWG can be configured with up to 12 output channels. The different configurations possible are explained in the 5.3 System Overview, page 33. In all configurations the channels are always synchronized and share the same sample clock. Each channel has its own output stage and therefore amplitude and offset are independent and can be set per channel.

There are two types of output configuration options:

- DC Output (standard): This is a differential DC-coupled output stage with variable amplitude control, with up to 1.3 Vpp amplitude and 0.5 V offset in a ±1.15 V window. Bandwidth is limited to work in the first Nyquist zone at maximum sample rate. To use this output in single ended mode, just use the '+' output and attach a high-quality 50 ohm terminator in the '-' output.
- Direct Output (optional): This is an AC-coupled output, with up to 600 mVpp amplitude, optimized for high bandwidth and dynamic range and excellent linearity. Although it is basically designed to be used as a single-ended output (keeping the unused output properly terminated), both '+' and '-' outputs can be used as two opposite-phase outputs if they are connected to impedance-matched loads. Usable BW covers the second Nyquist zone for all the Proteus models even at the maximum sampling rate.

5.5.1 Direct Mode

In the direct mode the signal being generated is coming from the onboard arbitrary waveform memory. Each part of the unit has a DDR4 module where the arbitrary waveforms are stored. When generating in the direct mode the data stored in the DDR4 is transmitted to the DAC and then to the channel output. When there are 2 channels per part the channels share the same waveform memory. The channels can read from the same segment simultaneously.

5.6 Channel Dependency

As explained in 5.3 System Overview, page 33 the AWG module consists of a maximum of two DACs with up to two channels per DAC. There are certain dependencies between the channels that need to be taken into consideration when using the instrument.

5.6.1 Inter-Part Channel

The inter-part dependencies relate to dependencies between channels on different DACs.

5.6.2 Dependencies

Clock System

The clock system is common to all channels, so they are always synchronized and share the same sampling rate.

Trigger Source Level

The trigger source level of each trigger input is common to all channels.

5.6.3 Intra-Part Channel Dependencies

The Intra-part dependencies relate to two channels in the same part. Channels in the same part have the same dependencies as channels in different parts with the addition of the segment table.

Segment Table

Each part has a single segment table that is shared between the two channels. However, each channel can access the segment table independently. This means that the channels can simultaneously generate the same segment from the segment table e.g. both channels generate segment 1. This results in efficient memory usage as there is no need to download the same

waveform twice. Alternatively, each channel can generate a different segment from the segment table e.g. channel 1 generates segment 10 and channel 2 generates segment 3. Refer to 6.4 Arbitrary Waveform Segments, page 42.

5.7 Triggers

While the Proteus system offers versatile waveform creation capabilities these would not be very effective without the ability to tightly control when and how the waveforms start and stop. For this purpose, the Proteus system offers an extremely flexible and sophisticated triggering system that control the start and stop of the waveforms.

The Proteus AWG responds to various trigger sources such as: external trigger signal from the TRIG1 And TRIG2 inputs, Internal trigger generator with programmable trigger period, and BUS trigger for triggering via the controlling PC using software commands.

The trigger source level for TRIG 1 and TRIG 2 inputs is programmed per trigger source and is common to all channels. All other trigger source attributes are independent and can be different for each channel. This means that user can set different trigger parameters for each channel on the same trigger input. In addition, trigger signals are used to both enable and abort waveform or task generation.

5.8 Function Mode

As mentioned in 5.3 System Overview, page 33 each part of the Proteus AWG has a DDR4 module that contains the arbitrary waveform memory of that part. The waveform memory is where the waveforms that are to be generated are stored. The duration of the generated waveform is limited by the size of the waveform memory.

One can use the entire memory for a single waveform or split the length to smaller segments. In this case, many waveforms can be stored in the same memory and replayed, one at a time, when recalled to the output.

There are two function modes, Arbitrary mode, and Task mode, that enable generating the waveforms stored in the memory.

5.8.1 Arbitrary Mode

In arbitrary mode the waveforms that are stored in the memory can be generated one at a time by selecting the segment to be generated. This mode is used when there is no prior knowledge to the order in which the segments should be generated. The selection can be done either by a software command or by external signal if the DJ option is installed.

For a more detailed explanation on the Arbitrary mode refer to 6 Arbitrary Mode, page 40.

5.8.2 Task Mode

The other option of playing out the segments is using the Task mode. Task mode enables generating sequences of segments in a predefined order. The user creates a Task table where each task defines numerous parameters such as the segment to generate, loop counter values, condition signals, advancement parameters, and the next task once the current task is done.

One Task table with up to 64K tasks can be defined per channel. In addition to the Task table the user can define a Scenario table. Each line in the Scenario table holds a pointer to a task. The default scenario table contains a single line which points to the first task of the task table. There can be up to 1K lines in the Scenario table.

The figure below describes the workflow of the Task mode. The first task in each sequence of tasks is the reference starting point. Note, a single task can be a sequence. The sequence of tasks is performed until an END state is reached. After this state the next line in the Scenario table is executed, this is repeated until all lines in the scenario table are executed.

For a more detailed explanation on the Task mode please refer to 7 Task Mode, page 46.

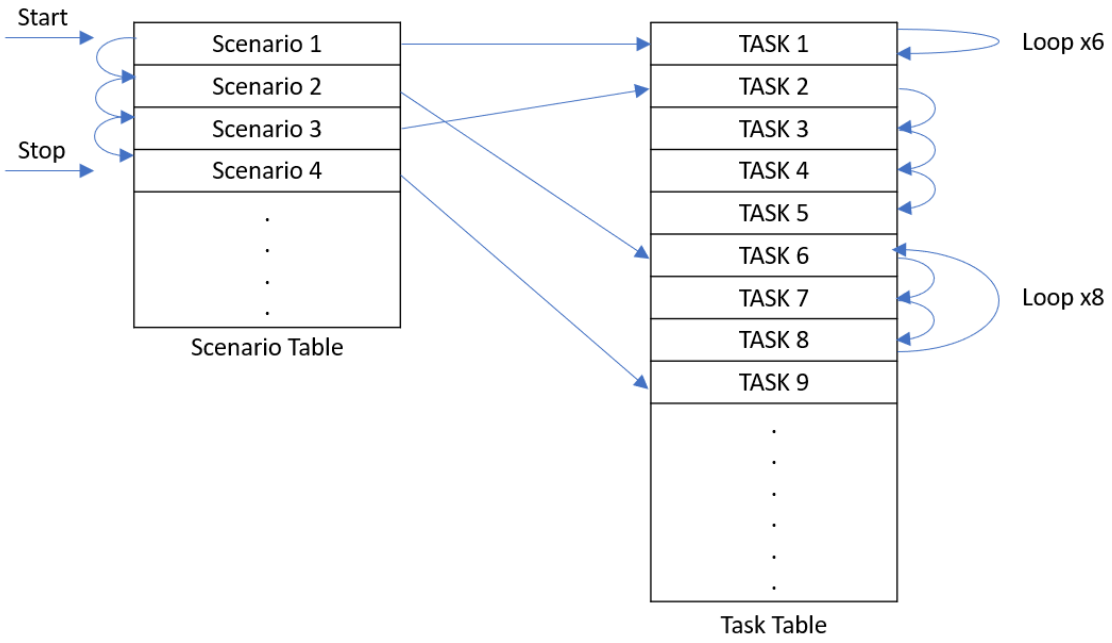

Figure 5.4 Task Mode

5.9 Markers

The Proteus AWG offers additional digital output signals called markers that are synchronized to the analog channel outputs. These can be used as clock signals or control signal for peripheral equipment. The markers data is separate from the waveform data and does not reduce the number of DAC bits available. The markers data is defined per segment and must therefore be identical to the segment length.

The number of markers varies depending on the model, as is shown in Table 2.1 Ordering Information, page 18. The number of markers are divided evenly among the channels, e.g., for the 2 channel 4 marker models each channel can have two markers M1, M2.

5.10 Dynamic Segment Control

The dynamic jump control option (DJ) integrates a 20-pin MDR connector in an additional PXI slot. The 20-pin connector has 2 bits for channel select, 1 bit for valid and 10 bits for data. Hence it is possible to select one of 1024 waveform segments to be generated on any of the channels. Having

the dynamic control feature, in effect, can serve as replacement of the task table where the real-time application can decide when and for how long a waveform will be generated. Refer to 12 Appendix , page 77 for a pin description.

5.11 Transceiver

For many of today's applications an advanced arbitrary waveform generator is just a part of the required solution. The waveforms that need to be generated vary depending on input signals from the environment. This type of conditional waveform generation requires not only generating signals but also capturing signals. For this reason, the Proteus series offers an option to transform the arbitrary waveform generator to an arbitrary waveform transceiver or AWT. The Proteus AWT integrates both a DAC and ADC in one system, controlled by a single FPGA for optimal synchronization and minimum latency.

The AWT option, offers an ADC with up to 9 GHz of analog bandwidth and a sampling rate of up to 5.4GS/s in single channel mode or up to 2.7GS/s in dual channel mode. The data captured by the ADC can either be streamed to the PC or stored on the internal waveform memory. When stored in the waveform memory the data can then be transferred to the PC for analysis or can be processed on the on-board FPGA for conditional waveform generation. For more details please refer to the Digitizer section of this manual.

5.12 Streaming

One of the primary concerns in any application that requires an AWG is the duration of the signal or scenario that needs to be generated. Traditionally the playtime duration is determined by the available waveform memory, the sampling rate, and the sequencing capabilities of the AWG. In addition, the entire waveform data must be downloaded to the AWG before waveform generation can begin.

The Proteus AWG offers up to 16GS of waveform memory and extremely powerful task mode that is sufficient for most application. However, e.g., radar applications require even longer playtimes. In addition, there are applications like quantum communication where the waveform data cannot be downloaded to the AWG prior to generation and has to be continuously generated.

For applications such as these, the Proteus series instruments offers the capability to continuously transfer waveform data from the controlling PC to the device.

There are two types of methods to transfer the data depending on the data type. Data that has already been created and is stored in a large file and data that is being continuously generated by another process. To distinguish between the two, the latter is referred to as dynamic streaming and the former as file streaming.

When streaming data, the controlling PC must be able to deliver the data faster than it is being generated by the instrument. This means that the hardware, software, and interface used are critical in order to achieve maximum throughput.

Note

The Proteus Benchtop communicate through a PCIe GEN3 4 lanes, with a throughput of 3.94 GB/s. Considering the encoding scheme overhead (20%) the maximum throughput that can be achieved is ~3.15 GB/s.

Regardless of the streaming type, to achieve optimal data throughput the waveform data should be transferred to the controlling PC RAM. This is to optimize the transfer speed as reading from the RAM is faster than from the PC hard drive.

The data management and synchronization is done using a dedicated API that is provided to the user and runs on the controlling PC. In dynamic streaming mode, the API will provide a pointer to a location in the RAM where the waveform data should be written. When using file streaming the file path should be provided to the API and the API will manage the file transfer. For more details concerning streaming refer to 5.12 Streaming, page 38.

Important

In streaming mode marker outputs are disabled to maximize throughput.

6 Arbitrary Mode

6.1 Introduction

The Proteus Arbitrary Mode is the most direct way to generate a waveform. Waveforms downloaded to segments in the generator's waveform memory can be played back at any sampling rate within the limits of the specific unit. The Proteus family of AWGs implements the "true-arb" architecture. The "True-Arb" architecture is the most flexible and accurate way to generate waveforms numerically. In this architecture, sampling rate is variable within a range and samples are read from the waveform memory in a purely sequential way. In the Proteus platform those samples can be organized in different ways depending on the waveform generation mode being used. Samples are processed in a variety of manners depending on the generation mode before being fed to the DAC. Depending on the model, Proteus modules can incorporate two or four channels with sample rates up to 1.25GS/s, 2.5 GS/s or 9 GS/s. Waveforms generated by each channel can be defined independently although all of them share the same final sampling rate.

6.2 Waveform Memory

The Proteus AWG stores waveforms in a DDR4 memory, see figure below. This memory also keeps other information such as marker states (see 8 Markers, page 53) and task and scenario tables (see 7 Task Mode, page 46). Samples are read in groups from the DDR so the overall transfer speed, measured is samples per second, is the same than the sampling frequency applied to the DAC, or a submultiple of it when interpolation is active. The maximum size of the DDR memory depends on the sampling rate of the model. The 1.25GS/s and 2/5GS/s models can incorporate up to 8G samples of memory for each part. The 9 GS/s incorporates up to 16G samples of memory per part. Although each bank of DDR4 waveform memory is physically associated to some specific part, the waveform memory can be freely accessed by the different channels (in the case of 2 channels per part) i.e. the two channels can read the same memory segment simultaneously or each channel can read a different segment.

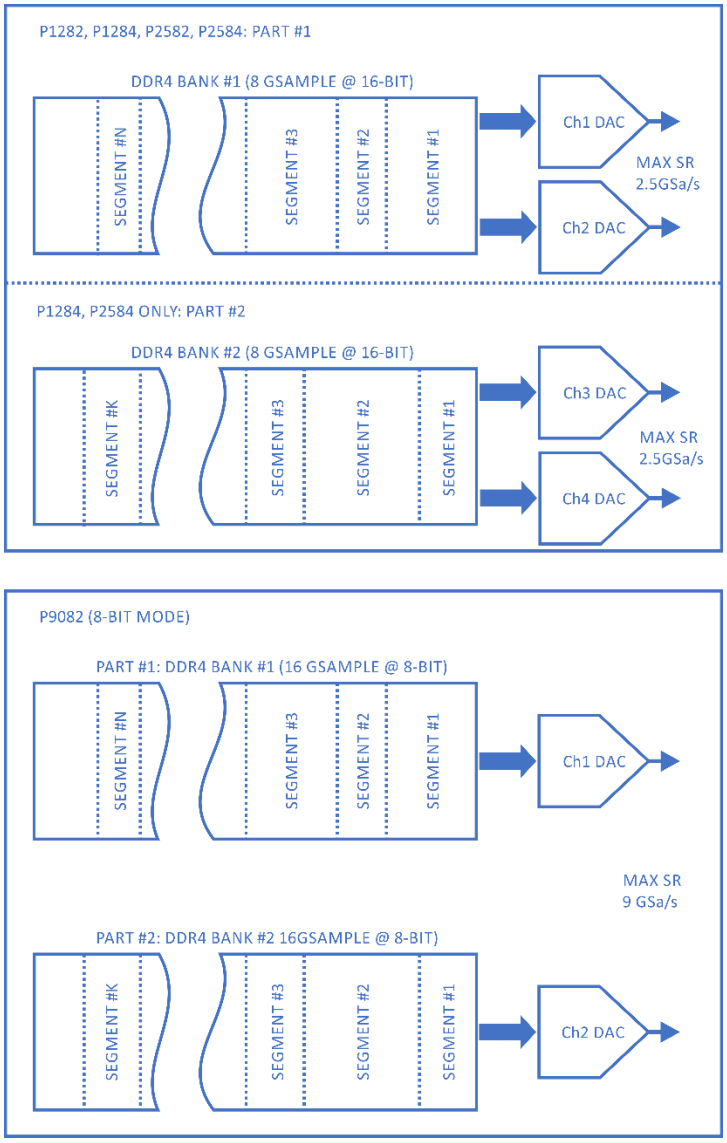

Figure 6.1 Waveform Memory

The internal organization of the waveform memory is based in grouping multiple samples in a 72-bit wide basic word (see below figure). This word carries either 4x16-bit samples or 8x8-bit samples (9GHz model). The additional 8 bits are used to carry two marker states (0/1) for the markers (up to 4 markers per channel) associated to the analog output channel. Marker behavior and set-up is described in section 8 Markers, page 53. Eight (8) 72-bit sample/marker groups are read in parallel from the DDR, so 32 16-bit samples or 64 8-bit samples are read simultaneously. The length (in samples) for all waveforms stored in the waveform memory must be a multiple of this number, known as waveform granularity. Optionally, waveform granularity can be reduced by half to 16 or 32 samples respectively. Lower granularity values provide more flexibility and accuracy when defining waveforms. Waveforms stored in the DDR must have a minimum length as well to be use for generation. For the 16-bit Proteus models, minimum length is 1024 samples while for the 8-bit models, minimum length is 2048 samples. Waveforms are stored in waveform segments within the waveform memory. For details, see section 6.4 Arbitrary Waveform Segments, page 42.

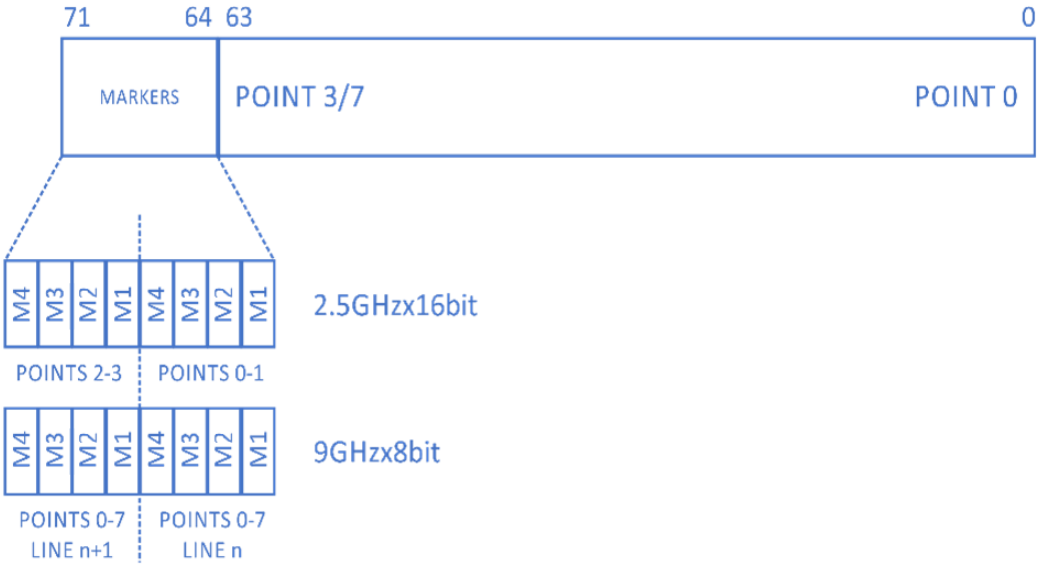

Figure 6.2 Waveform Memory Organization

6.3 Channel Dependency

The different channels in each Proteus module or group, share the waveform memory and sampling clock. Other than that, they operate in a basically independent manner. Segments, task, and scenario tables are independently defined for each channel so there is no restrictions regarding segment length or sequencing alignment between channels unless this is required by the test being carried out.

6.4 Arbitrary Waveform Segments

Waveform memory can be shared by multiple waveforms assigned to different segments. Segments are typically sections of the DDR4 memory holding a unique waveform. As any waveform, they must match the general requirements for minimum waveform length and granularity (see section 6.2 Waveform Memory, page 40). Segments may be used to store multiple waveforms in the waveform memory so they can be selected for generation at any moment without having to download the waveform to the Proteus unit every time it is needed. They can also be used in sequences to synthesize complex waveforms in a more efficient manner (see 7 Task Mode, page 46 for details). Finally, up to 1024 segments can be selected in real-time through a front panel connector in the optional DJ1/2 Dynamic Sequencing mode.

The characteristics of each segment is stored in a table associated to each channel called the Segment Table. This table can be defined and maintained though SCPI commands, IVI driver calls or through the WDS software. Segments can be created or deleted by adding or deleting entries into the segment table. These are the basic characteristics of regular segments:

- The maximum number of entries in the segment table for each channel is 64K (64 x 1024).
- •There is no limit for the size of a segment other than the available free waveform memory.

- Segments are identified by a unique integer number (1-64K).
- Segments characteristics (segment # and size) must be defined before downloading waveforms to them.
- The whole waveform (or a section of it) for any segment can be update at any moment, even if the generator is outputting that particular segment, without interrupting seamless arbitrary waveform generation.
- One or more entries in the segment table can be deleted freeing the associated waveform memory. This physical memory will be eventually reassigned when some new segment with the same or shorter length is defined.

6.5 Types

Regular segments stored in the DDR4 memory are convenient for most situations. When used in regular sequences, the next segment is read immediately after the end of the current segment iteration. In some event-generated jumps, this means that the time between the event and the actual instant the next waveform starts to be generated may be long and variable as it may depend on the relative timing of the event respect to that of the current segment. Even when setting up "immediate" jumping, time may be long and variable as the DDR4 memory takes time to be reconfigured for the next segment, and samples are transferred in chunks of up to 128 samples. In order to handle this issue, the Proteus platform allows users to store all or part of time-critical segments in a smaller size SRAM. Doing so, switching to the next waveform can be done independently of the DDR4 waveform memory constraints and enjoy much faster and more predictable jumps resulting in a much better trigger jitter performance.

Segments can be classified in three types in the Proteus platform:

- Regular Segments: These are implemented in the large DDR4 memory.
- Fast Short Segments: These segments are fully stored in the internal fast SRAM. Minimum size for short segments is 224 samples for the 9 GS/s units and 64 samples for all others.
- Fast Segments: Only the first samples are stored in the internal SRAM while the rest of the waveform is stored in the big DDR4 memory. When switching to a new fast segment, the first set of samples is read from the SRAM and they start to be fed to the DAC while regular DDR4 memory is set up for the new segment. Minimum size for short segments is 224 samples for the 9 GS/s units and 64 samples for all others.

The maximum number of fast and/or short segments that can be defined for each channel is 128. The maximum length such a segment stored in the SRAM is 8K samples (8x 1024).

6.6 Writing

Segments in the waveform memory can be loaded with waveform data through the appropriate sequence of SCPI commands and data formats. Waveforms can be downloaded in one single transfer process or divided into multiple transfers with arbitrary length sections. In fact, for extremely long waveforms, waveforms cannot be downloaded with a single transfer as the binary data block format does not support transferring blocks of data larger than 999,999,999 bytes (almost 1GByte). The reason for this is the format of the IEEE Std 488.2 binary data block format used along with the :TRACe:DATA command:

:TRACe:DATA #41280<binary_block>

As shown, above, the number of bytes to be transferred is defined by the integer number in ASCII characters before the binary data, and the size of the very same number depends of the previous #N sequence, where N is the a single digit number in ASCII format with the digits that must be read in ASCII format. Therefore, the maximum number of bytes in that transfer can only be expressed with a 9-digit integer. In order to handle waveforms with arbitrary length, waveforms can be split in different sections with supported lengths and be sent in a sequence. As waveform data can be overwritten (or edited) at any time, even while the very same data is being sent to the DAC for conversion, it is also useful being able to transfer just portions of the waveform when just a portion of the waveform must be updated. Finally, splitting the waveform in multiple sections can be used to update the GUI of the control SW during long transfers. Although transfer rates supported by the PCIe bus allow to download 1 G sample in under one second, sometimes data may be downloaded as it is calculated and calculation time may be quite long so the application may be stuck during this process unless data calculation and transfer is interrupted from time to time. This is a complete sequence of commands/actions required to successfully download a waveform to a segment in a given Proteus unit.

1. Select the channel for download (command :INST:CHAN:SEL{1|2|3|4})
2. Create the segment if not already created (:TRAC:DEF <SEG_NUMBER>,<SEG_LENGTH>)
3. Select the segment for download. Not necessary if next target for waveform data is the last segment created in step #2.
4. Download the section of the waveform. Section size is embedded in the binary block header (:TRAC:DATA[<OFFSET>,]#<HEADER><BINARY_BLOCK>)
5. Go to step #4 until the complete section has been downloaded.

The above sequence reflects the most general case. To make downloads easier in many cases, the pointer for the next sample to be downloaded is set to 0 (first sample in the segment) right after selecting or creating a segment. This pointer is updated after successfully downloading a given number of samples.

6.7 Reading

Waveforms can be read from the internal waveform memory in a very similar manner to the way they are written. The sequence of reading a waveform is the same as step 1 to 4 in writing a waveform, refer to section 6.6 Writing, page 43. However, unlike the writing process where the size of the segment is previously defined and the size for each transfer is specified (in bytes) as part of the binary block header, the reading process requires two extra steps in order to define the data to be read:

6. Determine the total size of the segment to be read in case is not already known (command :TRAC:DEF?).

The waveform data received from the Proteus unit is formatted in the same way binary blocks for waveform downloads are:

#Nn..n<binary_block>

6.8 Streaming

AWGs typically generate signals based on waveforms stored in the waveform memory. These waveforms may be used directly or after a series of processing steps (sequencing, interpolation, real-time filtering, digital up-conversion). Although the waveform memory may be very big, it can be insufficient for some applications. In some other cases, waveforms must be calculated in real-time as they are being generated. In order to support such scenarios, the Proteus platform supports real-time streaming from the PCIe backplane (part of the PXIe bus). Proteus provides PCIe Gen3 8-lanes wide. This interface supports an overall raw data rate of around 50 Gbps. This results in a seamless conversion rate of over 6GS/s for one AWG channel using 8-bit samples. The available BW must be shared among channels in the same or different modules.

7 Task Mode

7.1 Introduction

The Proteus AWG platform supports an advanced waveform generation mode named Task Mode. Within Task Mode, users can define a table for each channel made of up to 65,536 entries. Each entry fully specifies the way a given segment is going to be generated. One segment can be assigned to any number of task entries or not any entry. Tasks can be simple, independent single segment generation schemes, or they may be part of a complex sequence with synchronous or asynchronous, conditional, or unconditional jumps to other tasks depending on events defined for each task. Tasks also define what to output during idle periods (before the task enabling event or after the current task has been completed and the generator is waiting for the next jumping event).

Each task points to a single segment and the same segment may be pointed by different tasks. For the P128X and P258x models, segments are shared by channel pairs (ch1/ch2 and Ch3/ch4 pairs and so on) so even tasks from different channel can point to the same segment.

In addition to the Task Table, the Proteus AWG platform incorporates an additional task control layer implemented in the Scenario table. This table is made of up to 1024 entries. Each entry points to a task (which in fact can be the initial task of a complex sequence) so “sequences of sequences” can be easily defined (and modified) without having to edit the task table.

Both tables, Task and Scenario, can be defined entry by entry from the WDS (Wave Design Studio) GUI (Graphical User Interface) or through SCPI (Standard Commands for Programmable Instruments) commands. These commands allow for the definition in a readable format of each entry and the corresponding parameters one by one, or they can be handled in a more efficient, fast, and compact way by transferring the whole or parts of those tables in binary format to the device.

7.2 Task Table

There is a unique Task table defined for each channel. Each table can hold up to 65,536 entries. There are two types of tasks:

- Single task: Segment, number of loops, enable and disable events, jumping mode and next task (if any) to be generated are defined. This means that single tasks can be member of a complex sequence.
- Sequence task: There are three subtypes of Sequence task: *StartSequence*, *InsideSequence*, and *EndSequence*. Sequence tasks behaves identically to Single tasks, but they can be grouped as an independent entity that can be looped any number of times (or indefinitely). The purpose of this task type is to simplify the creation of complex sequences, where sections of it must be repeated a given number of times. Otherwise, each repetition should be implemented by additional entries in the Task Table (one for each loop), consuming resources in terms of table space, table creation code and download time. The location of tasks associated to a given segment within the task table is not limited. This means that segments part of the same group do not have to be contiguous and that the “single” and “sequence” tasks can be located anywhere in the table.

Sequencing is the most important functionality added by the Task Mode. Sequences can be linear , so one task can be executed after the other as they are listed in the Task Table, or they can be generated in a non-linear way, as the next task to be executed after the completion of the current task is one of the task attributes that can be defined by the user. Jumping from one task to the other can be controlled by events generated by software (i.e. the ***TRG** SCPI command) or different internal or external trigger signals. Jump destination can be deterministic to a single predefined task or it may be selected among several choices depending on the event generating the jump allowing for conditional branching.

The best way to handle such a complex, flexible and powerful sequencing scheme, is by thinking of it as a state machine where tasks are the states and events control the transition between states. A very institutive way to design and visualize such state machines are state diagrams. An alternative representation of the sequencer functionality is a flow chart. Flow charts are probably the best tool to handle the Task Mode in Proteus as it directly shows the behavior of the sequencer in the time-domain. From now on, flow charts will be used to illustrate and define the Task Table functionality. The following graph shows the type of blocks relevant to this situation.

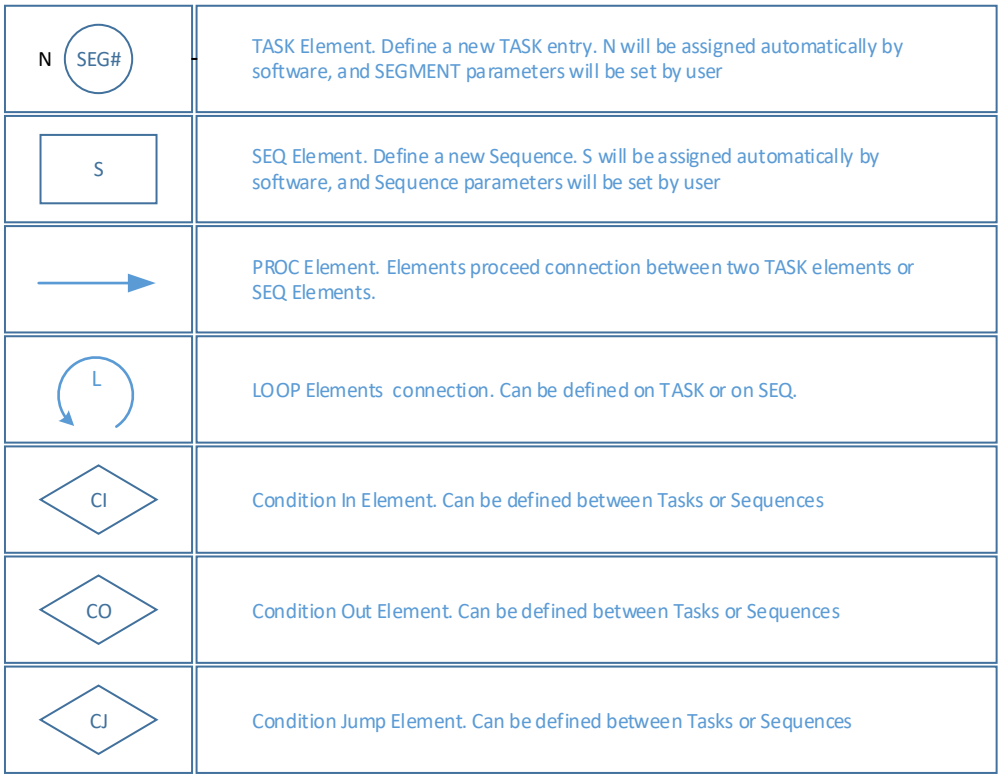

Figure 7.1 Type of Blocks Implemented by the Task Table

Additionally, a given task can also define the behavior of the output channel during the “idle” state, the period before the task itself is enabled by the designated event or after the completion of the current task and before jumping to the next task as set by the *Next task Delay* parameter. The aborting conditions (so the current task is terminated) can be also defined for each task. Finally, the number of repetition loops for the associated segment can be set form 0 (continuous) to 1,048,576. Jump can take place as soon as the Aborting event is received (Immediately) or after the current loop is finished (Eventually).

Figure 7.2 below shows an example of a task table using the blocks shown in Figure 7.1 Type of Blocks Implemented by the Task Table

above. The green numbers indicate the task numbers, the blue numbers in the circle indicates the segment number, CI indicates a Condition In (e.g. Enable signal), CO indicates Condition Out (e.g. Conditional jump).

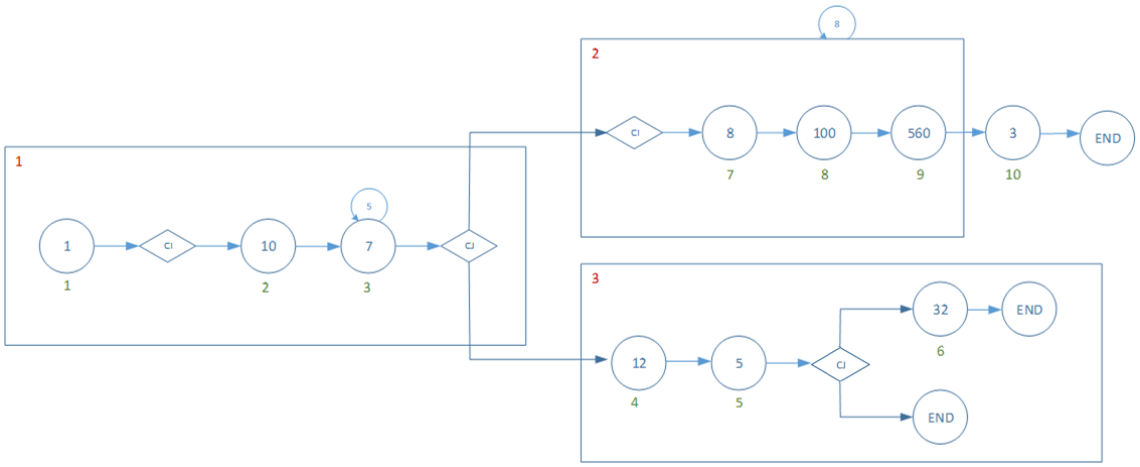

Figure 7.2 Flowchart for an Example Task Table

7.3 Task Table Parameters

Tasks are defined by a series of parameters associated to each task. Although all these parameters are included in the Task Table for each entry, not all of them may be active as there are some interdependencies. Below are the parameters, their possible values and states, and a description of the corresponding functionality. Refer also to WSD, SCENARIO COMPOSER, Task in the WSD User Manual.

- **Task No.**: This is just the number of the entry in the table. It is automatically assigned when a new task is defined. Task can be selected by using this unique number.
- **Task State**: It indicates the type of task for that entry. It allows for the definition of groups of tasks that can be used together as a single entity so looping for it can be defined independently of the member tasks. These are the possible choices:
  - **Single**: An independent task not being part of a group of tasks.
  - **StartSequence**: This type of task defines the beginning of a group of tasks to be used as a group. The loops for the group must be defined for these tasks in the corresponding parameter (“Sequence Loops”).
  - **InsideSequence**: This type of task defines a task within the grouped tasks.
  - **EndSequence**: This sequence defines the final task within the group. After terminating this task, the group will be looped again from the StartSequence task until the defined number of loops have been completed. Once this condition is matched, the next task will be controlled by the jump definition parameters for this task.
- **Task Loops**: This is the number of times for the task to be looped. It can go from 0 (continuous looping) until 1,048,576 times.

- **Sequence Loops**: This is the number of times for the grouped tasks to be looped. It can go from 0 (continuous looping) until 1,048,576 times. This parameter is only active when Task State is set to StartSequence.
- **Seg Number**: This is the segment number pointed by the current task. This will be the segment fed to the DAC for generation. The same segment can be referenced by any number of tasks. Channel 1&2 and 3&4 in the P128X and P258X models share the same segments for each pair so the same segments can be referenced by tasks in Task Tables for each channel.
- **Idle Waveform**: It states the behavior of the output before the effective generation of the waveform segment pointed by the current task takes place, the so called "idle state". The "idle state" can be active while the sequencer is waiting for the enabling event or when a delay is forced through the Task Delay parameter. These are the possible choices:
  - **DC**: This is just a user-defined fixed voltage specified in DAC levels (0-255 for the P908X and 0-65,535 for the P128X and P258X models).
  - **FirstPoint**: This is a fixed voltage level specified by the value of the first sample in the segment pointed by the current task.
  - **CurrentSeg**: The segment pointed by the current task will be generated during the "idle state".
- **DC Value**: This is the user-defined fixed voltage specified in DAC levels (0-255 for the P908X and 0-65,535 for the P128X and P258X models) for the Idle Waveform state while in the "DC" mode.

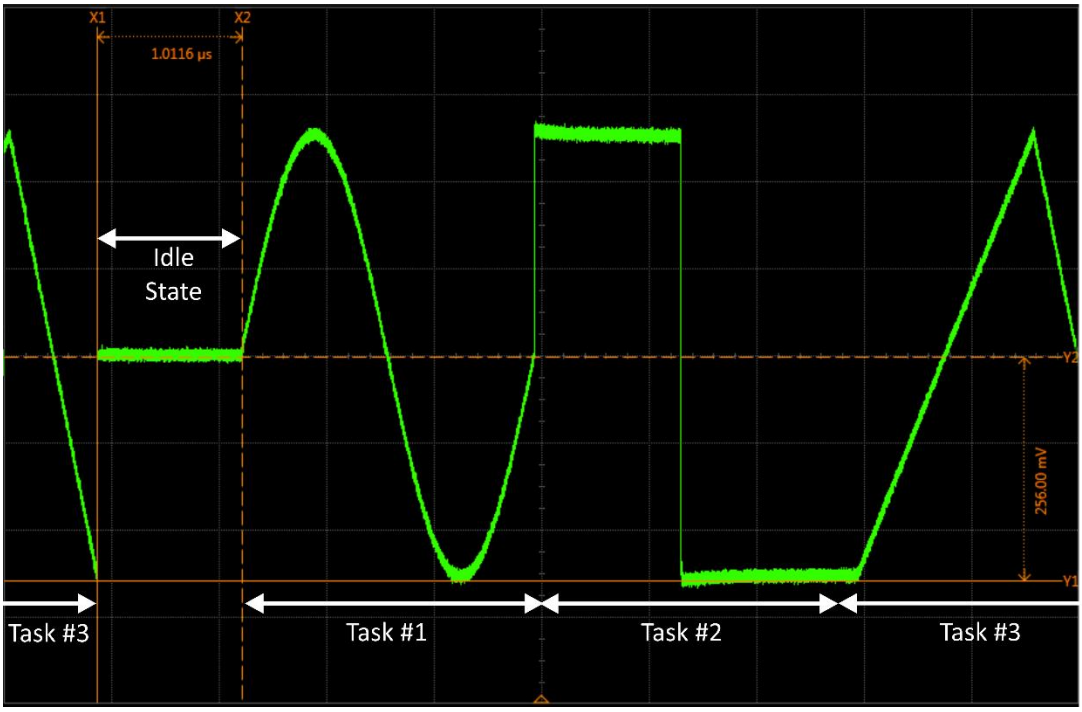

Figure 7.3 DC Level Idle State Associated to Task #1

- **Enabling Signal**: The following sources can be used to initiate the execution of a given task:
  - **None**: The task is initiated immediately (after the time set buy the Task Delay parameter).

- **ExternTrig1**: External Trigger input 1. Trigger 1 settings are set independently.
- **ExternTrig2**: External Trigger input 2. Trigger 2 settings are set independently.
- **InternTrig**: Internal Trigger Source.
- **CPU**: Bus trigger through SCPI commands (*TRG).
- **FeedbackTrig**: Trigger from the digitizer block in the optional AWT (decision block). The trigger conditions are set independently.
- **HwControl**: Using the optional DJ1/2/3 option.

- **Aborting Signal**:
  - **None**: The task is terminated immediately after the number of loops defined in the Task Loops parameter.
  - **ExternTrig1**: External Trigger input 1. Trigger 1 settings are set independently.
  - **ExternTrig2**: External Trigger input 2. Trigger 2 settings are set independently.
  - **InternTrig**: Internal Trigger Source.
  - **CPU**: Abort signal through SCPI commands (*TRG).
  - **FeedbackTrig**: Trigger from the digitizer block in the optional AWT (decision block) associated to the digitizer section (AWT) . The trigger conditions are set independently.
  - **AnyExternTrig**: Any of the external trigger inputs (Trigger 1 and Trigger 2) when activated according to the respective settings set independently.
- **Jump Mode**: Jumping can be synchronous or asynchronous with the generation associated to the task. According to the expected behavior, Jump Mode can be set to one of these two modes:
  - **Eventually**: After detecting a valid trigger signal for jumping, jump is carried out after full play back of the current loop of the associated segment.
  - **Immediately**: This is used in conjunction with an abort signal or conditional jump. Jump is carried out as fast as possible after detection of the jumping conditions. The latency between a valid trigger to a change in the output is determined by the system delay of the unit and varies depending on the sampling clock. However as long as the system settings are constant the latency time is deterministic (not including the trigger jitter).

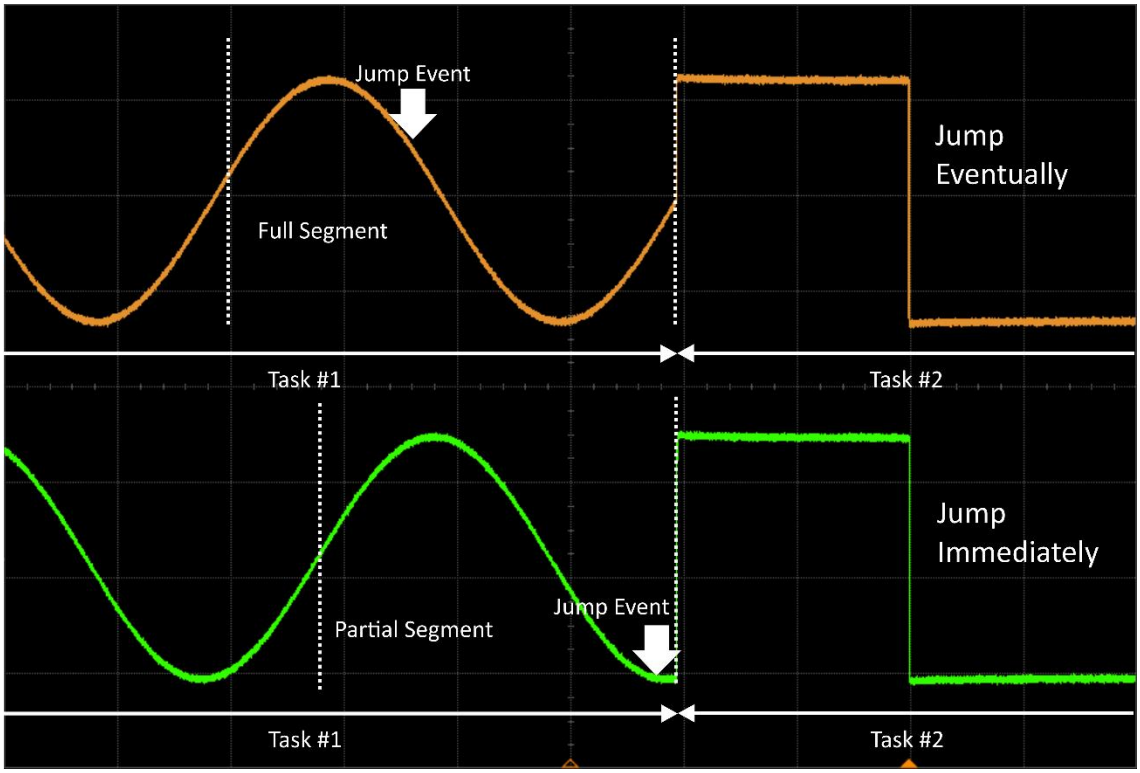

Figure 7.4 Jump Eventually (Top) and Jump Immediately (Bottom)

- **Jump Destination**:
  - **Next1Task**: Next task as designated by the Next task 1 parameter.
  - **FeedbackTrigValue**: Task number set by the Feed-Back Trigger coming from the decision block associated to the digitizer section in the optional AWT.
  - **SwitchNext1Next2**: Next task will be defined by either the Next Task 1 (TRIG1) or the Next Task 2 (TRIG2) parameter depending on the first valid trigger event detected from either the External Trigger 1 or External Trigger 2 sources.
- **Next Task 1**: Task 1 number for the Next1Task and SwitchNext1Next2 jump destination.
- **Next Task 2**: Task 2 number for the SwitchNext1Next2 jump destination.
- **Task Delay**: This is a delay expressed in an integer number of sample periods to effectively start the current task. During this period, the output is in the “idle state”.
- **Loop with Trigger**: When a task has an enable signal and a task loop count larger than 1 this selects whether a trigger outputs all of the task loops or just one loop. For example, a task is looped three times and TRIG1 is the enable signal, when the Loop with Trigger is disabled, a single trigger is required to advance to the next task. When the Loop with trigger is enabled three triggers are required to advance to the next task.

7.4 Task Table Limitations

While the task mode offers powerful and flexible sequencing features there are certain limitations that the user must adhere to when programming the task table.

7.4.1 Conditional Jump

When using the conditional jump capability, the destination task must meet the following conditions:

1. The segment must be a Fast Short Segment see 6.5 Types, page 43.
2. There cannot be an enable signal, an abort signal, a task delay, or a task loop greater than 1.
3. Task state cannot be end of sequence.
4. Jump destination must be Next1Task.

7.4.2 Segment Transitions

When transitioning between segments it is not possible to transition from a Fast-Short Segment to a regular segment. Only Fast Segments can transition to regular segment.

7.4.3 Trigger Signal

When using a trigger signal in task mode in conjunction with jump mode eventually there is a minimum hold off time that must be observed in order for the unit to detect the trigger. The trigger signal must be at least 64 sample clocks after the end of the segment in the 9GS/s units and 16 sample clocks after the end of segments in all the other units.

7.5 Scenario Table

The scenario table implements an upper layer of task execution control. Each entry in the Scenario Table point to a given task and specifies a number of loops (repetitions) for each entry. As tasks pointed by the Scenario table can be sequences, this scheme allows for the definition of “sequence of sequences” kind of scenarios. The last task in the sequence must contain “Next Scenario” as its Jump Destination definition. In this way, control is returned to the Scenario Table so it can repeat the same task, if the number of loops set for this entry is not completed or jump to the next entry. The Scenario Table is defined independently for each channel and can keep up to 1024 entries. When the Scenario Task is not defined, there is a “default scenario” launching task # 1.

8 Markers

8.1 Introduction

The Proteus series of instruments offers programmable digital output signals that are synchronized to the main analog outputs. These signals are referred to as markers. The purpose of these markers is to provide auxiliary outputs, that are fully synchronized with the output waveforms, for control of peripheral equipment or as additional digital data stream. Each channel output can have between 1 – 4 corresponding marker outputs depending on the model and the configuration. The number of markers are divided evenly among the channels, e.g., for the 2 channel 4 marker models each channel can have two markers M1, M2.

8.2 Marker Control

Control of the markers is done by addressing each marker separately. Each marker output can be programmed to have a unique set of data, amplitude, DC offset and time delay. The amplitude and DC offset of each marker can be set using the relevant voltage and offset SCPI commands or in WDS. The markers are aligned so that the skew in time between the analog channels and the markers is kept to a minimum. In addition, it is possible for the user to add delay in time for each marker with respect to the analog channel outputs. The delay can be set in either sample clock periods or in units of time.

8.3 Programming the Markers

When a segment is defined in the segment table it has its corresponding wave data and marker data. Every time a segment is generated the corresponding waveform and markers are generated. There is a defined relationship between waveform data and marker data. There is one byte of markers data per eight bytes of waveform data. The ratio between the number of wave points and marker points depends on the Proteus model.

8.3.1 9 GS/s Model

For the 9GS/s model there is one markers-point per eight waveform-points, and the sampling rate of the markers is 1/8 the sampling rate of the waveform.

For example, if a segment of 4096 waveform points is defined, then it is necessary to download:

- 4096 bytes of waveform data that hold 4096 waveform points
- 512 bytes of markers data that hold 512 markers-points.
- For every byte of marker data, the routing is as follows:

Table 8.1 Byte of Marker Data 9 GS/S Models Channel 1/2

Bit 0	Marker 1
Bit 1	Marker 2
Bit 2	Marker 3
Bit 3	Marker 4
Bit 4	N/A
Bit 5	N/A

Bit 6	N/A
Bit 7	N/A

Example

Assume that we have defined a segment of 32 waveform points. The waveform data consists of 32 bytes (1 byte per waveform point). Let's download waveform-data that represents one cycle of sinusoid waveform.

Reminder

The 32 points segment is for example purposes. The minimum segment size for 9GS/s model is 256 points.

The markers data consists of 4 bytes (1 byte per marker point for 8 waveform points). Let's download the four markers bytes: 0x01, 0x02, 0x04 and 0x08.

It means that during the first eight ticks of the sampling clock marker 1 is high, during the next eight ticks marker 2 is high and so forth.

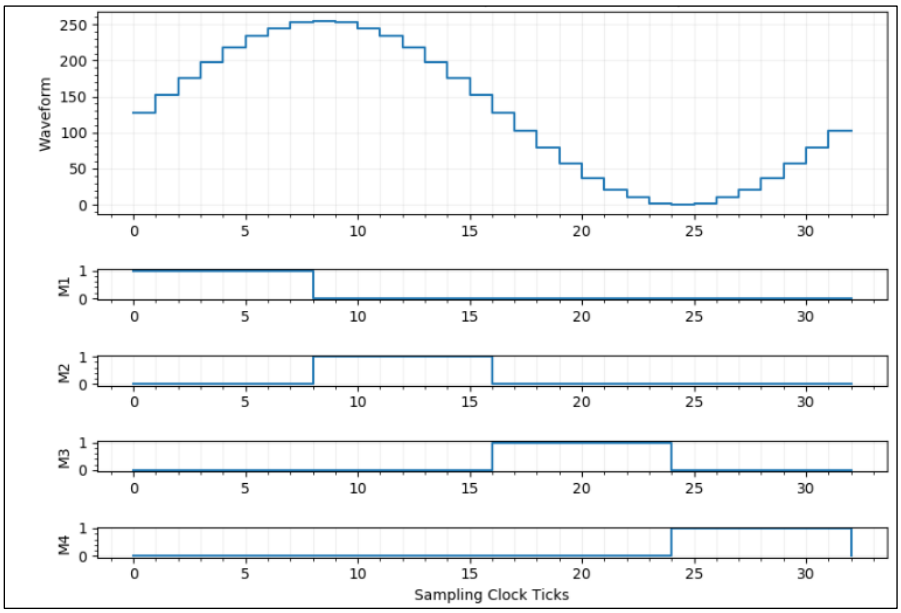

Figure 8.1 9 GS/s Model - 32 Waveform Points and 4 Marker Points

Segment Data

Waveform Data	
Index	Byte (decimal) value
0	128
1	152
2	176
3	198
4	218
5	234
6	245
7	253
8	255
9	253
10	245
11	234
12	218
13	198
14	176
15	152
16	128
17	103
18	79
19	57
20	37
21	21
22	10
23	2
24	0
25	2
26	10
27	21
28	37
29	57
30	79
31	103

Markers Data	
Index	Byte (decimal) value
0	1
1	2
2	4
3	8

Figure 8.2 Segment Data

8.3.2 1.25 GS/s and 2.5 GS/s Models

For the 1.25 GS/s and 2.5 GS/s models there is one markers-point per two waveform-points, and the sampling rate of the markers is half the sampling rate of the waveform.

In this case each waveform point occupies 2-bytes, and each byte of marker-data holds two marker-points.

For example, if a segment of 2048 waveform points is defined, then it is necessary to download:

- 4096 bytes of waveform data that hold 2048 waveform points
- 512 bytes of markers data that hold 1024 markers-points.
- For every byte of marker data, the routing is as follows:

Table 8.2 Byte of Marker Data 1.25 GS/S and 2.5 GS/S Models

Bit 0	Marker 1
Bit 1	Marker 2
Bit 2	N/A
Bit 3	N/A
Bit 4	Marker 1
Bit 5	Marker 2

Bit 6	N/A
Bit 7	N/A

Example

Assume that we have a P2582M model, and we defined a segment of 8 waveform points. The waveform data consists of 16 bytes (2 bytes per waveform point). Let's download waveform-data that represents one cycle of sinusoid waveform.

> **Reminder**
> The 8 points segment is for example purposes. The minimum segment size for 1.25GS/s or 2.5GS/s models is 64 points.

As there are 2 waveform points per marker point, the markers data consists of 4 marker points or 2 bytes (2 marker points per byte). Let's download the two markers bytes: 0x21, 0x84.

It means that during the first two ticks of the sampling clock marker 1 is high, during the next two ticks marker 2 is high and so forth.

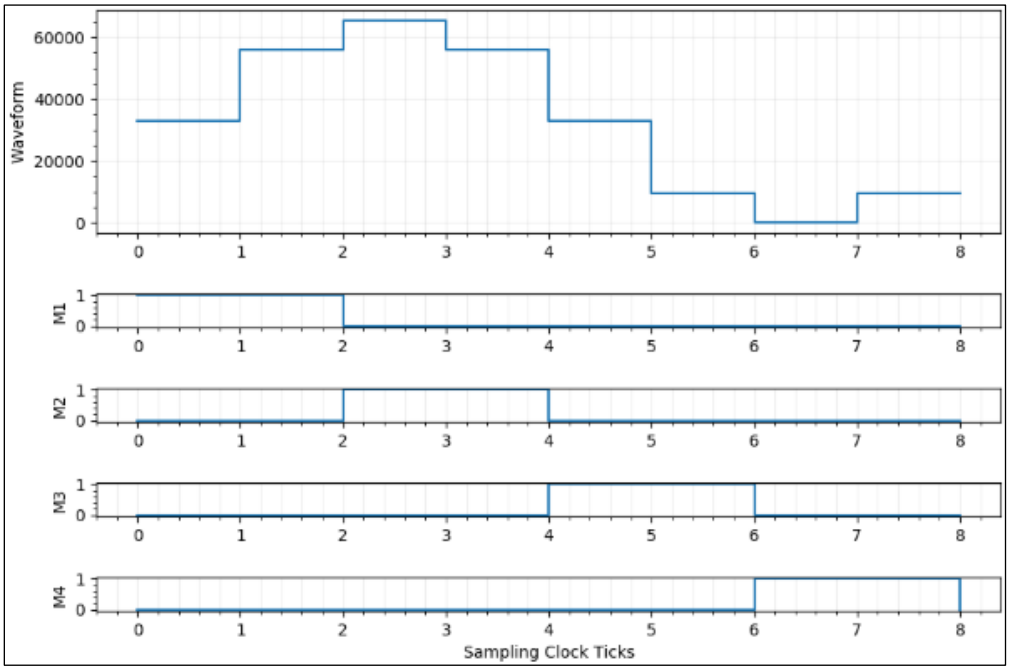

Figure 8.3 P2582M Model 8 Waveform Points and 4 Marker Points

Segment Data

Waveform Data

Index	Word (decimal) value
0	32768
1	55938
2	65535
3	55938
4	32768
5	9597
6	0
7	9597

Markers Data

Index	Byte (decimal) Value
0	33
1	132

Figure 8.4 Segment Data

9 Triggering System

9.1 Introduction

The ability to program and control what is being generated from the AWG requires two basic functionalities. The first is being able to program the memory segments with the desired waveform data to be generated, as was explained in chapter 6 Arbitrary Mode, page 40. The second functionality is being able to control which segment or task is to be played out and when.

The simplest way to generate a waveform or task table is simply to program it in advance, as explained in the Arbitrary and Task mode chapters. The waveform or task table will be generated continuously once the output is switched on. However, in many applications, the exact timing of the generation of each waveform or task needs to be controlled. For this reason, there is a triggering system, where various signals, internal or external can be used to apply certain conditions to the waveform generation.

In this chapter we will explain how the triggering system works and its capabilities.

9.2 Trigger Run Modes

As explained previously the Proteus device has two operation modes, Arbitrary and Task. Trigger functionality is applied differently depending on the operation mode of the instrument.

9.3 Arbitrary Mode

When operating in arbitrary mode the Proteus device has two run modes, continuous and trigger.

In continuous run mode the waveform stored in the selected segment is available at the output terminals when the channel output is turned on. The selected segment is played continuously and will continue until a different segment is selected, the output is turned off or the run mode is set to trigger.

Once the device is set to trigger run mode the trigger is armed and is sensitive to the input signal or bus commands depending on the trigger source. At the channel output an idle waveform is generated. The idle waveform can be selected by the user and the available options are explained in section 9.7 Output Channel Trigger Settings, page 62.

9.4 Task Mode

When the Proteus device is set to task mode, the waveforms are generated according to the task table. As explained in the Task mode chapter the task table is made up of different tasks. Each task in the task table contains multiple parameters, such as enable signal, abort signal, and jump condition that define the trigger functionality for the given task. Therefore, in task mode there is no selected run mode but rather each task is played out according the conditions defined.

9.5 Trigger Source

The Proteus AWG option can be initiated to produce waveform functions from several trigger sources.

- Trigger In 1 labelled TRIG 1 (WDS, Trigger, ExternTrig1).
- Trigger In 2 labelled TRIG 2 (WDS, Trigger, ExternTrig1).
- Bus commands that are applied to the instrument (WDS, Trigger, CPU).
- Internal Trigger (WDS, Trigger, InternTrig).
- Digitizer, (Option AWT) (WDS, Trigger, FeedbackTrig).
- Dynamic Jump connector (Option DJ) (WDS, Trigger, HwControl).

9.5.1 TRIG 1/2

When activating the external TRIG 1 or TRIG 2 trigger source, every valid signal that is applied to the input connector is stimulating the Proteus device. To define the condition for a valid signal, it is necessary to program the trigger level and trigger slope. The trigger level defines the necessary voltage level that the trigger signal needs to cross for it to stimulate the instrument. While the trigger slope defines whether the trigger input is sensitive to a positive transition or negative transition. The trigger level is defined per trigger input and is common to all channels.

9.5.2 Bus

When selecting Bus as a trigger source, trigger commands from a remote interface are accepted by the instrument.

9.5.3 Abort (Jump) Mode

Until now we have discussed scenarios where the Proteus device is idle and is then triggered. However, there are many applications where the device receives a valid trigger while a segment is being generated. The abort mode parameter enables the user to control exactly how the instrument reacts in such a case.

There are two setting options for the abort mode:

- Eventually – In Eventually mode, the first valid trigger that is received is accepted by the device. However, the current segment that is played is completed before the trigger action is initiated. Any consecutive triggers that are received while the segment is being played are ignored.
- Immediately – In Immediately mode, the instrument does not complete playing the current segment but performs the trigger action on the next clock cycle. Any consecutive valid trigger that is received is accepted and the programmed trigger action is executed.

9.5.4 Internal Trigger

An additional source for trigger generation is the internal trigger. There are two operating modes in this state:

- In periodic mode, an internal time counter is generating trigger pulses every specific time elapsed. It is the user responsibility to ensure that the generated trigger will not interrupt wave generation before its end.

- In delay mode, the user sets the number of clocks which will generate a trigger after the wave generation ends. TBD

9.5.5 Digitizer (AWT)

When configured with the AWT option, the digitizer can be programmed so that a valid signal triggers the instrument.

9.5.6 Dynamic Jump Connector (DJ)

When configured with the DJ option, the valid signal on the dynamic jump connector can be set to trigger the instrument.

9.6 Trigger Source Attributes

For each trigger source the user can program certain attributes. These attributes constitute what is the trigger state and what is a valid trigger signal. All the trigger source attributes except trigger level are channel dependent and can be different for each of the instrument's channels.

The trigger source attributes are described in the following paragraphs.

9.6.1 TRIG 1/2

External trigger inputs TRIG1 and TRIG2 have the following attributes:

- Trigger State – Enables or disables the trigger state for the specified channel. When trigger state is ON the trigger input is armed for the active channel. When turned off the trigger input is inactive and ignores all trigger signals.
- Trigger Type – Selects between the type of trigger signal. Edge defines the valid trigger on the transition of the trigger signal. Gate type trigger signal outputs the waveforms on a stable gate level between two gate transitions. The gate opens on the first positive trigger transition and closes on the next negative transition.
- Trigger Polarity – When the selected trigger type is Edge user can set whether trigger is initiated on the rising edge or falling edge of the trigger signal

Trigger Pulse Detect Width – The trigger pulse detect width sets the width of a valid trigger signal in units of time. User sets a time interval during which the trigger signal valid level must be kept in order for the trigger signal to be valid.

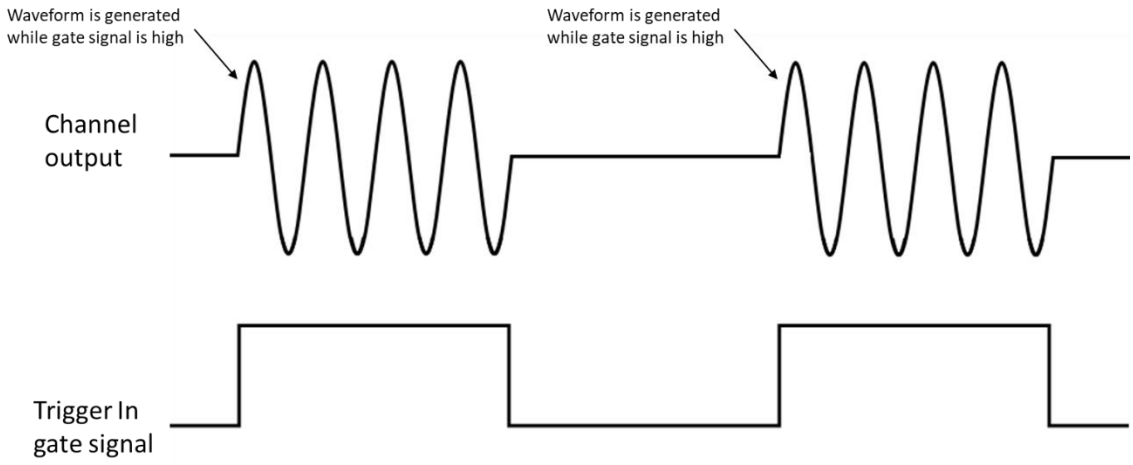

Figure 9.1 Output Signal with Gate Type Trigger

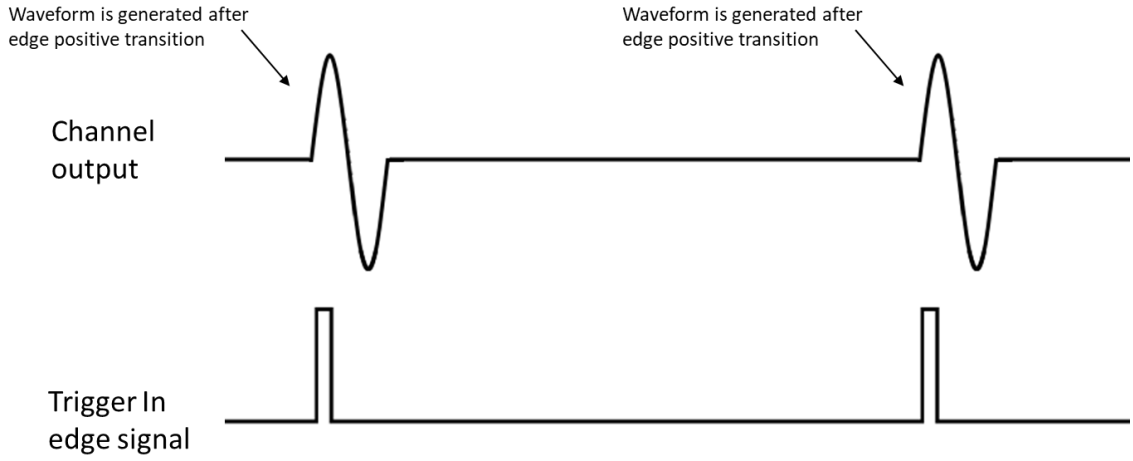

Figure 9.2 Output Signal with Positive Edge Type Trigger

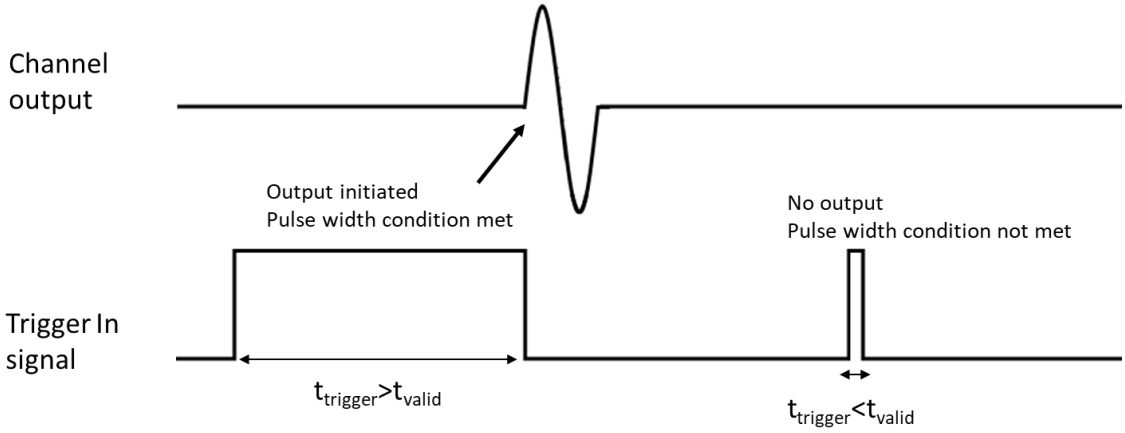

Figure 9.3 Outputs Behavior with Pulse Detect Width Set to Time t_{valid}

9.6.2 Internal Trigger

The internal trigger generator operates as a free running asynchronous trigger generator. It may be used for applications that require periodical and constant generation of output cycles, or to replace external trigger devices. The following attributes can be programmed:

- Trigger State - Enables or disables the trigger state for the specified channel. When trigger state is ON the internal trigger generator is active channel. When turned off the internal trigger generator is inactive.
- Trigger Period – Sets the time period between triggers for the internal trigger generator.

Note

- In order to prevent errors, the period of the internal trigger must be larger than the period of the output waveform.

9.7 Output Channel Trigger Settings

The trigger source attributes define the state of the trigger source and the conditions for a valid trigger signal. Once those are defined it is necessary to define the behavior of the instrument once a valid trigger signal is received. The following paragraph describe the parameters that can be defined to control the instrument response to a valid trigger signal.

9.7.1 Enable (Start) Source

The enable source defines which trigger source starts the waveform generation. User can set any one of the available trigger sources as the source for initiating waveform generation.

Note

In arbitrary mode one of the trigger sources must be set as the enable source. If set to none the unit will not output any waveform in trigger mode.

9.7.2 Disable (Abort) Source

The disable source defines which trigger source aborts the waveform generation. User can set any one of the available trigger sources as the source for aborting waveform generation.

9.7.3 Idle Waveform

When the channel output is waiting for a trigger the output must still generate a waveform. This waveform is referred to as the idle waveform. User can select between 3 idle waveforms:

1. DC – the output is a DC waveform. The DC level can be programmed as explained in the following paragraph.
2. FirstPoint – The output is a DC waveform of a level that is equivalent to the first point of the segment to be generated.
3. CurrentSeg – The output is the waveform programmed to the current segment.

9.7.4 DC Level

When the idle waveform is set to DC, the DC level parameter enables the user to program the required DC level of the idle DC waveform. The level is programmed in value of DAC bits and enables the users to select any DC level as the idle level of the channel output while waiting for a trigger.

9.7.5 Loops Count

Once the Proteus device receives a valid trigger signal to generate a segment the user can program the number of times that segment is to be repeated. The number of repetitions, or loops, is set in the Loops Count parameter.

Note
When the loops count is set to 0 the segment will be repeated infinitely until it is aborted.

9.7.6 Low trigger Jitter (LTJ Option)

A trigger signal, whether it comes from an external source or from an interface command, is routed through electrical circuits. These circuits cause a small delay known as system delay. System delay cannot be eliminated completely. System delay is a factor that must be considered when applying a trigger signal. It defines the time that will lapse from a valid trigger edge or software command to the instant that the output reacts.

In case of a trigger signal that is asynchronous to the device system clock, an additional variant delay called trigger jitter is added to the system delay. The trigger jitter is defined as the variation in time of the triggered signal position with respect to the triggering signal.

Trigger jitter adds uncertainty to the generated signal. This can be a very critical parameter in many applications and experiments that need the generated signals to be very near or completely deterministic.

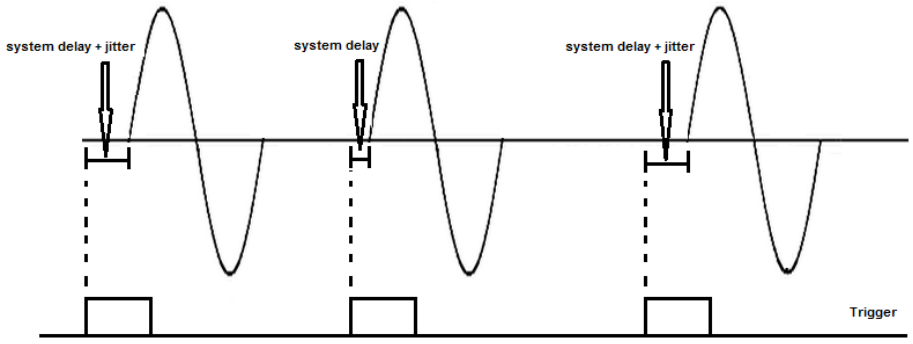

Figure 9.4 Trigger Jitter and System Delay

The Proteus series offers several options on how to minimize the trigger jitter. For asynchronous trigger signals there is the Low Trigger Jitter option. This option can be added when ordering your Proteus device. Using this option can reduce the trigger jitter by a factor of more than 10. To activate the option user simply needs to turn the low trigger jitter state to ON.

Note
Activating the low jitter option reduces the trigger jitter however the system delay is increased.

9.8 Minimizing Trigger Jitter

As discussed in the previous section when stimulating the Proteus device with a trigger that is asynchronous to the system clock, user can minimize the trigger jitter by enabling the low trigger jitter option. However, in many applications in order to minimize the trigger jitter even further the trigger signal and triggered instrument are synchronized.

One option is to feed the same reference signal to both triggering and triggered instruments. However, the Proteus device offers the CLK OUT signal. When this signal is used as the triggering device clock it guarantees the lowest attainable trigger jitter.

10 Remote Control

10.1 Introduction

The Proteus benchtop platform must be used in conjunction with the embedded host computer or an external connected host. There are three ways to program the device, the first being low-level programming of each individual parameter, using SCPI commands. The second alternative is to use WDS (Wave Design Studio) for high-level programming. WDS is a software package supplied with the device that enables full control and programming via a user-friendly graphical user interface. The third alternative is using application specific drivers, such IVI (Interchangeable Virtual Instrument) or LabVIEW drivers.

10.2 Wave Design Studio

The WDS is the latest in instrument control and signal creation software. It enables full remote control of Tabor's waveform generators and simplifies the creation of complex signals. With a powerful and intuitive graphical user interface WDS offers easy access and control of all the instruments features and capabilities. In addition to the standard waveform creation tools, WDS offers waveform creation add-ons for radar, and future microwave, RF, and general-purpose applications. Refer to Wave Design Studio (WDS) User Manual that can be downloaded from www.taborelec.com/downloads.

10.3 SCPI Programming

SCPI (Standard Commands for Programmable Instruments) is an ASCII-based instrument command language designed for test and measurement instruments. SCPI commands are based on a hierarchical structure, known as a tree system. In this system, associated commands are grouped together under a common node or root, consequently forming subsystems.

For a detailed explanation of how to program the instrument through SCPI commands please refer to the "Proteus Series Arbitrary Waveform Transceiver Programming Manual".

Idea

- Use the WDS command editor and log window (Menu > Options) to learn how to program the unit with SCPI commands. All SCPI commands are logged in the log window and the command editor enables sending specific SCPI commands to the instrument.

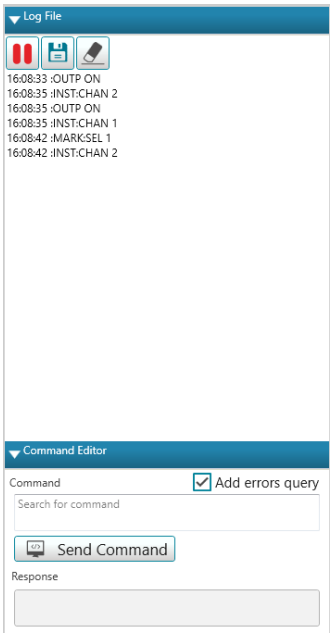

Figure 10.1 WDS Log Window and Command Editor

10.4 IVI Driver Programming

An alternative method for programming is using the IVI instrument driver. The IVI driver is an instrument driver specified by the IVI (Interchangeable Virtual Instrumentation) foundation, that follows a set of software routines that simplify the programming of test and measurement instruments. The IVI driver for the Proteus instrument is available on the CD supplied with your Proteus device or for download from the Tabor website.

11 Proteus Benchtop Specifications

11.1 Channels Characteristics

Table 11.1 Channels Characteristics

Channels Characteristics	P9082/4/6B	P2582/4/8/12B	P1282/4/8/12B
Number of Channels	2/4/6	2/4/8/12	2/4/8/12
Initial Skew	<20 ps		
Fine Delay			
Range	0 to 5 ns		
Resolution	5 ps		
Accuracy	±5 ps		
Coarse Delay			
Range	0 to wavelength		
Resolution	1 sample point		

11.2 Arbitrary Mode

Table 11.2 Arbitrary Mode

Arbitrary Mode	P9082/4/6B	P2582/4/8/12B	P1282/4/8/12B
Max. Sample Rate	9 GS/s	2.5 GS/s	1.25 GS
Resolution	Up to 16-bit (depending on model and mode)		
Max. Memory Size	Up to 16 GS	Up to 8 GS	
Number of Segments	64k		
Minimum Segment Length			
Normal	2048 points	1024 points	
Fast Segment	224 points	64 points	
Waveform Granularity			
Standard	64 points	32 points	32 points
Optional	32 points	16 points	16 points
Interpolation Modes	x1	x1, x2 and x4	

11.3 Task Mode

Table 11.3 Task Mode

Task Mode	
Task Table Length	64k tasks per channel
Task Loops	1M
Sequence	A sequence is defined as a continuous and looped series of tasks
Max. Number of Sequences	32k sequences
Sequence Loops	1M
Scenario	A scenario is defined as a continuous series of tasks/sequences
Max. Number of Scenarios	1k scenarios

11.4 Streaming (STM Option)

Table 11.4 Streaming (STM Option)

Streaming (STM Option)	
Max. Stream Rate	6 GS/s
Minimum PC Requirements	
CPU	i7
Internal Memory	32 GB
Operating System	Windows 10
Source	Internal / rear panel interfaces

11.5 Signal Purity

Table 11.5 Signal Purity

Signal Purity	DC Output	Direct Output
Harmonic Distortion[1]		
fout = 10 MHz - 200 MHz, Measured @ DC to 2 GHz	<-70 dBc (typ.)	<-70 dBc (typ.)
fout = 200 MHz ... 1.5 GHz, Measured @ DC to 4.5 GHz	<-60 dBc (typ.)	<-60 dBc (typ.)
fout = 1.5 GHz ... 4.5 GHz, Measured @ DC to 4.5 GHz	<-50 dBc (typ.)	<-50 dBc (typ.)
SFDR[2]		

fout = 10 MHz…500 MHz, Measured @ DC to 1.5 GHz	-80 dBc (typ.)	<-85 dBc (typ.)
fout = 500 MHz…4.5 GHz , Measured @ DC to 4.5 GHz	-70 dBc (typ.)	<-75 dBc (typ.)
Phase Noise (@10 kHz Offset)		
fout = 140.625 MHz	-134 dBc/Hz	
fout = 280.25 MHz	-128 dBc/Hz	
fout = 562.5 MHz	-122 dBc/Hz	
fout = 1.125 GHz	-116 dBc/Hz	
fout = 2.25 GHz	-110 dBc/Hz	
fout = 4.5 GHz	-104 dBc/Hz	

[1] SCLK=Max sample rate, amplitude = 400 mVpp, direct mode, measured using a balun

[2] SCLK=Max sample rate, amplitude = 400 mVpp, excluding SCLK/2-fout, measured using a balun.

11.6 DC Output

Table 11.6 DC Output

DC Output	
Connector	2 x SMA per channel
Output Type	Single-ended or differential, DC-coupled
Impedance	50 Ω (nom.)
Amplitude	50 mVp-p to 1.3 Vp-p
Amplitude Resolution	1 mV
DC Amplitude Accuracy	±(3 % of amplitude ±2 mV)
Voltage Window	±1.15 V
DC Offset	±0.5 V
Offset Resolution	10 mV
DC Offset Accuracy	± (3% of setting ±15 mV)
Skew Between Normal and Complement Outputs	0 ps
Rise/Fall Time (20% to 80%)	< 130 ps (typ.)
Instantaneous Bandwidth P128xB | P258xB | P908xB	625 MHz | 2.25 GHz | 4.5 GHz
Max. Usable Frequency P128xB | P258xB | P908xB	2nd Nyquist 1.25 GHz | 1.5 GHz | 4.5 GHz

Jitter (Peak-Peak)	<15 ps (typ.)
Overshoot	<5% (typ.)

11.7 Direct Output (Optional)

Table 11.7 Direct Output (Optional)

Direct Output (Optional)	
Connector	2 x SMA per channel
Output Type	Single-ended or differential, AC coupled
Impedance	50 Ω (nom.)
Amplitude	1 mVpp to 600 mVpp, single-ended into 50 Ω
Amplitude Resolution	1 mV
Amplitude Accuracy	±(3% of amplitude ±2 mV)
Rise/Fall Time (20% to 80%)	< 60 ps (typ.)
Instantaneous Bandwidth P128xB | P258xB | P908xB	 625 MHz | 1.25 GHz | 4.5 GHz
Max. Usable Frequency	2nd Nyquist
P128xB | P258xB | P908xB	1.25 GHz | 2.5 | 9 GHz

11.8 Sample Clock Output

Table 11.8 Sample Clock Output

Sample Clock Output	
Connector	1 x SMA
Impedance	50 Ω (nom.), AC coupled
Source	Selectable, internal synthesizer or sample clock input
Frequency Range	SCLK range
Output Amplitude	0.5 V to 1 V depending on SCLK

11.9 Sync Clock Output

Table 11.9 Sync Clock Output

Sync Clock Output	
Connector	1 x SMP
Impedance	LVCMOS
Amplitude	500 mVpp, typ.

Frequency P908xB P128xB, P258xB	 SCLK/32, SCLK/8
Waveform	Square
Rise/fall time (20% to 80%)	<150 ps

11.10 Marker Outputs

Table 11.10 Marker Outputs

Marker Outputs	
Connector	SMP
Number of Markers P1282B, P1284B P1288,P2582,P2584, P9082B P12812B P2588B, P9084B P25812B, P9086B	 4 8 12 16 24
Output Type	Single ended
Output Impedance	50 Ω (nom.)
Amplitude	
Voltage Window	±1.15 V
Level	32 mVpp to 1.2 Vpp (32 discrete levels)
Resolution	10 mVpp
Accuracy	±7%
Offset	
Range	±0.5 V
Resolution	10 mV
Accuracy	±(3% of setting ±15 mV)
Rise/fall time (20% to 80%)	<200 ps
Range	0 - waveform length
Resolution P128xB, P258xB P908xB	 2 pts 8 pts
Marker Delay	
Coarse Delay	
Range	0 to 2048 points

Resolution P128xB, P258xB P908xB	 8 points 32 points
Fine Delay	
Range	0 to 1.2 ns
Resolution	1 ps
Accuracy	15 ps

11.11 Reference Clock Output

Table 11.11 Reference Clock Output

Reference Clock Output	
Connector	1 x SMP
Source	Internal TCXO
Waveform	Square
Frequency	100 MHz or REF IN
Stability	+/- 2.5 PPM
Aging	+/- 1 PPM @ +25°C (per year)

11.12 Reference Clock Input

Table 11.12 Reference Clock Input

Reference Clock Input	
Connector	1 x SMP
Impedance	50 Ω, AC coupled (nom.)
Input Frequencies	10 MHz / 100 MHz selectable
Lock Range	± 1 MHz
Input Level	0.6 Vp-p to 1.7 Vp-p

11.13 Sample Clock Input

Table 11.13 Sample Clock Input

Sample Clock Input	
Connector	1 x SMA
Input Impedance	50 Ω nom, AC coupled
Frequency Range	SCLK range
Input Power Range	0 to 1 V

Damage Level	<0.5 V or >1.5 V

11.14 Trigger Inputs

Table 11.14 Trigger Inputs

Trigger Inputs	
Connector	2 x SMP
Input Impedance	10 kΩ or 50 Ω (nom), DC coupled, factory configured
Range	–5 V to +5 V
Threshold	±5 V
Resolution	100 mV
Sensitivity	200 mV
Jitter Standard P128xB, P258xB P908xB Low Trigger Jitter Opt.	 8 SCLK periods 32 SCLK periods SQRT(SCLK period^2 + 150e-12^2)
Latency / System Delay P128xB, P258xB P908xB	 <900 SCLK periods <2700 SCLK periods
Polarity	Positive or negative
Source	Selectable between channels
Input Impedance	10 kΩ or 50 Ω (nom.), DC coupled, factory configured
Max Toggle Frequency	50 MHz
Minimum Pulse Width	5 ns

11.15 Fast Segment Dynamic Control Input (Optional)

Table 11.15 Fast Segment Dynamic Control Input (Optional)

Fast Segment Dynamic Control Input (Optional)	
Input Signals	data 10bit, channel select 2 bit, valid 1 bit
Segments / Sequences	1024 (128 fast)
Data Rate	35 MHz
Minimum Latency (Dynamic Control Input to Direct Out)	
Fast Segment	<250 ns
Normal Segment	<1 µ
Input Level	LVTTL

Connector	D-SUB 9-Pin

11.16 Digitizer Characteristics (AWT Option)

Table 11.16 Digitizer Characteristics (AWT Option)

Digitizer Characteristics (AWT Option)	
Connector	SMA per channel
Number of Channels	1 or 2
Input Voltage Range	500 mVpp (full scale)
Input Voltage Offset	-2 V to +2 V
Input Frequency Range	9 GHz
Resolution	12 bits
Acquisition Memory	Up to max memory size
Sample Clock Sources	Internal or external
Internal Clock Source	Internal, external reference
Max Sampling Rate	5.4 GS/s in single channel mode 2.7 Gs/s in dual channel mode
Min Sampling Rate	1 GS/s
Clock Accuracy	<2 ppm
Impedance	50 Ω
Coupling	DC or AC (factory configured)
Trigger System	
Trigger Modes	Positive, negative edge
Trigger Sources	External, software, channel
Coupling	DC
Impedance	50 Ω (nominal)
Level Range	>± 2.5 V (nominal)
Frequency Range	DC to 65 MHz

11.17 FPGA Programming

Table 11.17 FPGA Programming

FPGA Programming	
FPGA Type	Xilinx Kintex UltraScale XCKU060 upgradeable to XCKU115
Modes	

Standard	Tabor standard built-in functionality
Decision Blocks	Built-in library of mathematical functions, modulation & digital filters
Shell	Open core providing all interfaces and configuration path to the user

11.18 Digital Upconverter

Table 11.18 Digital Upconverter

Digital Upconverter	
Modes	NCO only / digital upconverter
Sampling Rate	1 GS/s to max sample rate
Carrier Frequency	
Range	0 to 40% of sampling rate
Resolution	48 bit
Phase Range	0 to 360°
Phase Resolution	16 bit
All IQ Parameters	Same as arbitrary mode

11.19 General

Table 11.19 General

General	
Input Voltage Range	100 VAC to 264 VAC
Input Frequency Range	47 Hz to 63 Hz
Power Consumption:	550 W max.
Interfaces	
USB	front panel 1 x USB 3 host (type A) rear panel 2 x USB 3 host, (type A) rear panel 1 x USB 3 device, (type C)
Thunderbolt (Optional)	rear panel 1 x Thunderbolt 3
LAN (1000BASE-T)	rear panel 1 x RJ45 1000/100/10
SFP+ (Optional, Replaces RJ45)	rear panel 1 x SFP+ 10G optical
GPIB (Optional)	IEEE 488.2 – GPIB
HDMI	HDMI type A
Storage	120GB removable

Dimensions With Feet Without Feet	 440 X 175 x 330 mm (W x H x D) 440 X 190 x 330 mm (W x H x D)
Weight Without Package Shipping Weight	 7.5 kg 9 kg
Temperature Operating Storage	 0°C to +40°C -40°C to +70°C
Warm up Time	15 minutes
Humidity	85% RH, non-condensing
Safety	CE Marked, EC61010-1:2010
EMC	IEC 61326-1:2013
Calibration	2 years
Warranty	1 or 3 year warranty plans

12 Appendix D-Sub 9-Pin

The allowed voltage levels for the D-Sub connector are 0 - 5 V (TTL) (or 0-3.3 V CMOS) and must comply with VIH=1.17 V, VIL=0.63 V levels. Voltage levels below -0.5 V and above 6 V will damage the device.

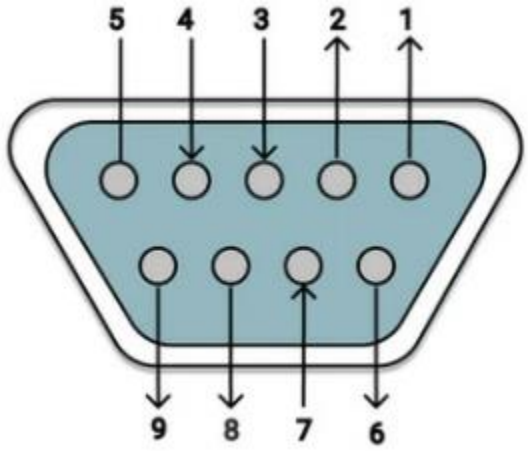

Figure 12.1 D-Sub 9-Pin Female Pin Numbering

Table 12.1 D-Sub 9-Pin Connector Pin Description

Pin	Description
1	Segment number LSB
2	Segment number
3	Segment number
4	Segment number
5	Segment number
6	Segment number MSB
7	Channel number LSB
8	Channel number MSB
9	Valid

13 Appendix Log File

The WDS provides a log file at C:\temp that provides all the communication between WDS and the device. If you encounter any issue, include this file when reporting to Tabor support.

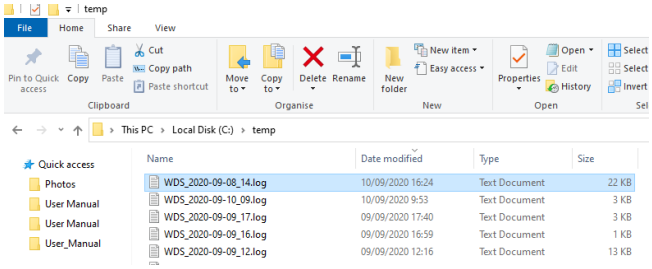

Figure 13.1 WDS Log File Folder

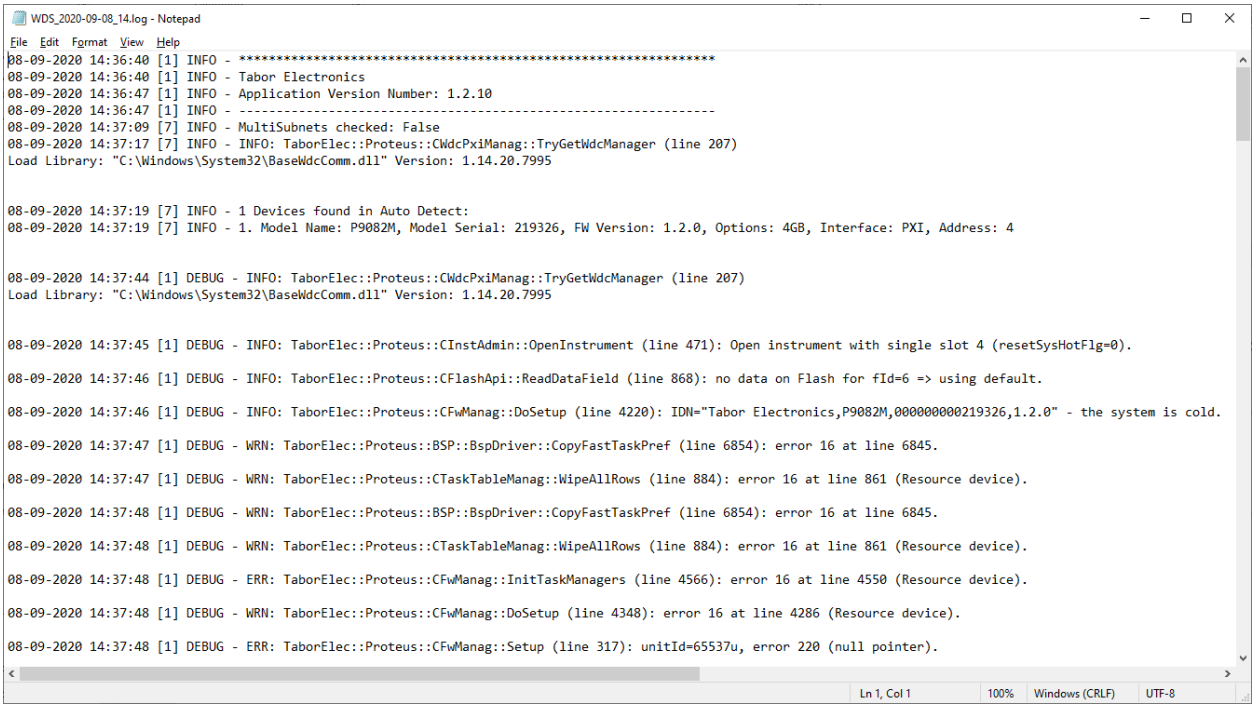

Figure 13.2 WDS Log File

14 Appendix Troubleshooting

14.1 Manually Installing Instrument Drivers

1. You should use the supplied USB Type C cable to connect the Proteus benchtop model to the PC. If the following screen is displayed with “No driver found”, then you have to install the USB2LAN driver manually.

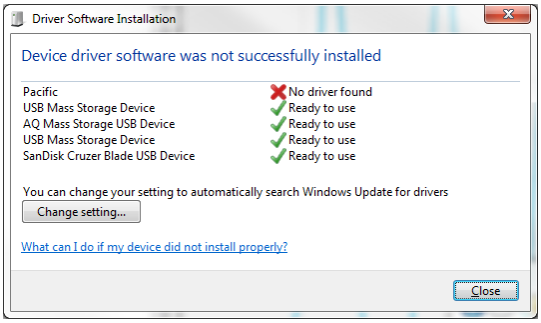

Figure 14.1 Driver Software Installation

2. Download the latest Proteus series USB2LAN device driver from www.taborelec.com/downloads. For Windows 10 64-bit use Aquantia_AQtion_USB_x64_v1.8.0.0.msi and for Windows 10 32-bit use Aquantia_AQtion_USB_x86_v1.8.0.0.msi.

3. Extract your file and double-click it to start the installation.

Figure 14.2 Aquantia Software License Agreement

4. Check “I accept..” and click Install. The installation starts.

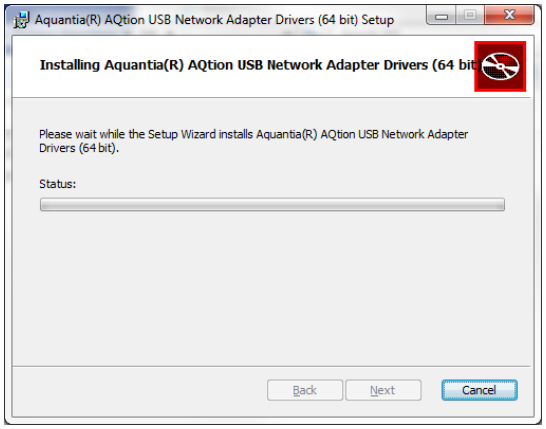

Figure 14.3 Installing Aquantia USB Network Adapter

5. The User Account Control dialog box will open. Click Yes.

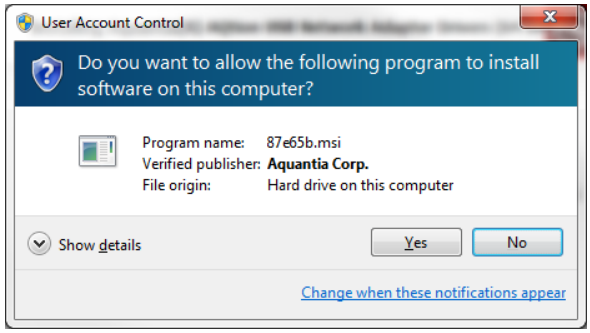

Figure 14.4 User Account Control

6. The Completed…Setup Wizard dialog box will open. Click Finish.

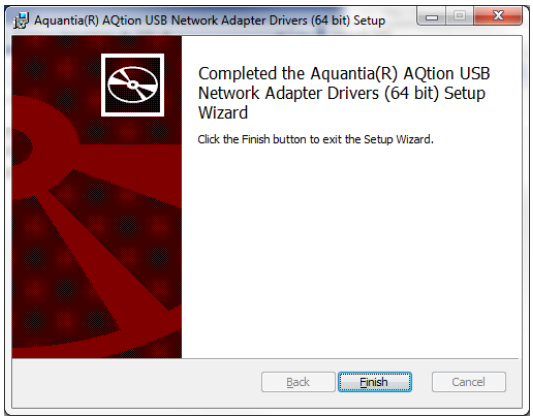

Figure 14.5 Completed … Setup Wizard

7. Open the Windows Device Manager to verify that under Network adapters that the “Aquanti AQtion USB to 5GbE Adapter” is installed properly.

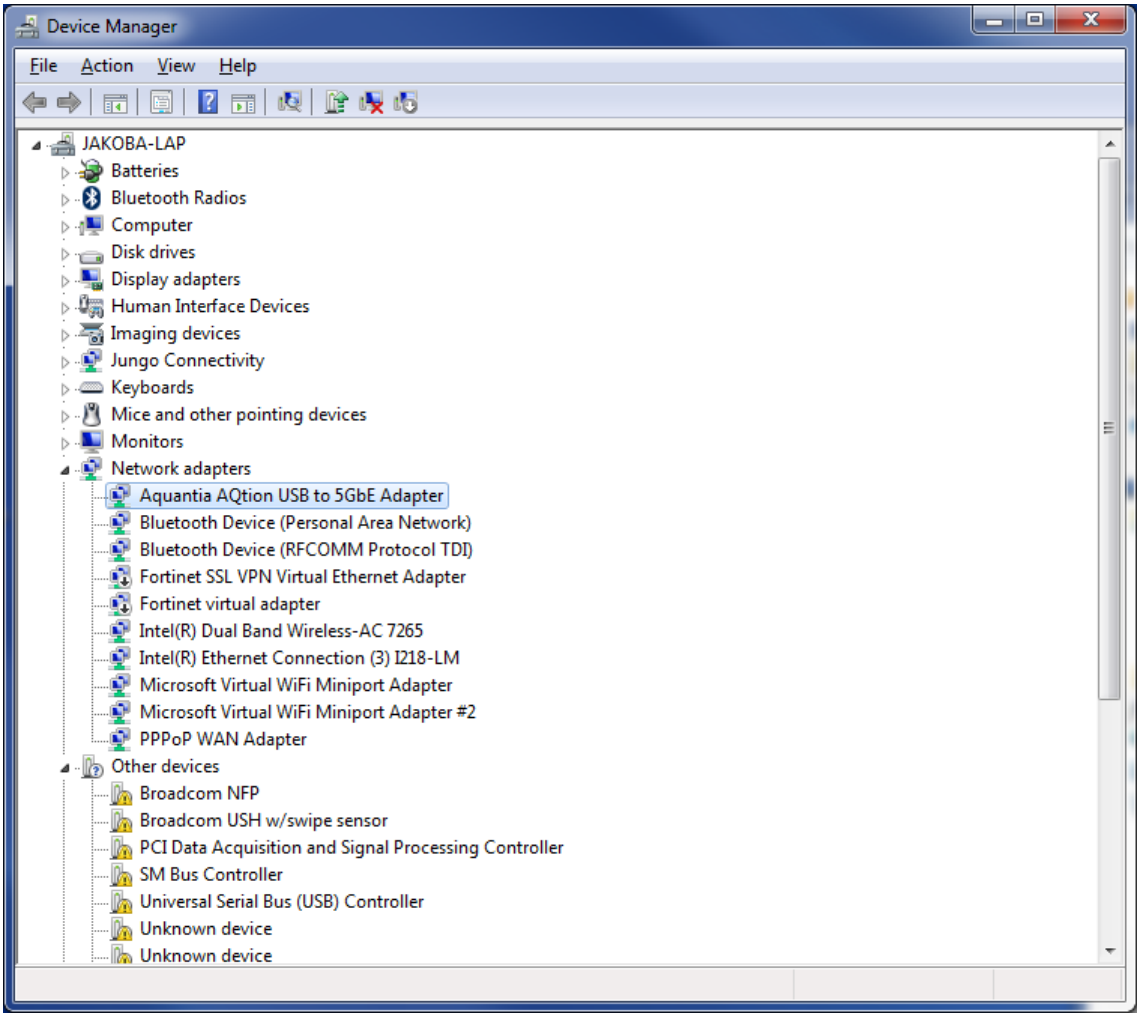

Figure 14.6 Device Manager

8. In the Aquanti AQtion USB to 5GbE Adapter Properties window the displayed device status should be: The device is working properly.

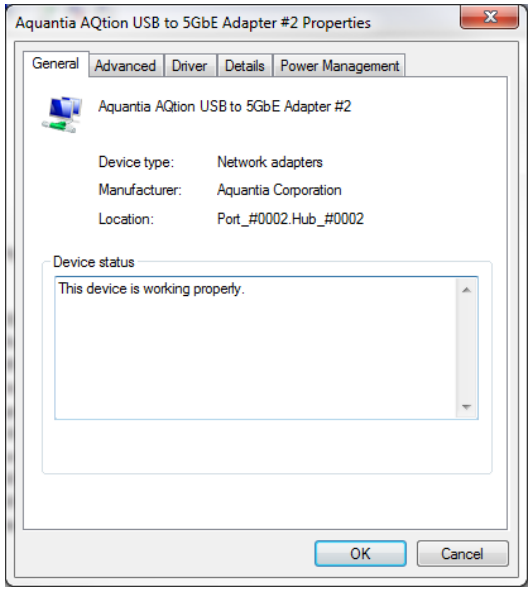

Figure 14.7 Aquantia USB2LAN Properties